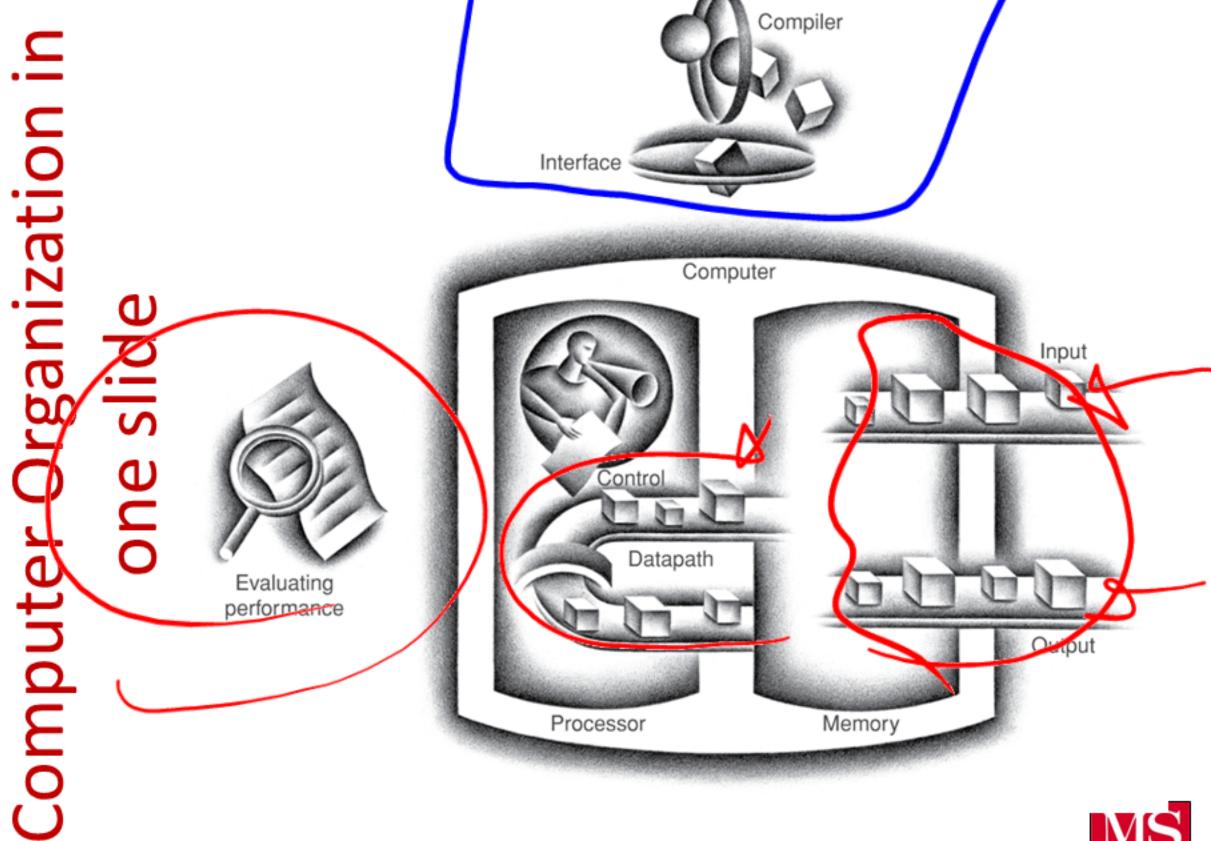
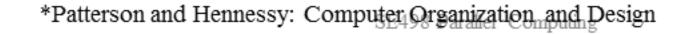


Parallel Hardware?

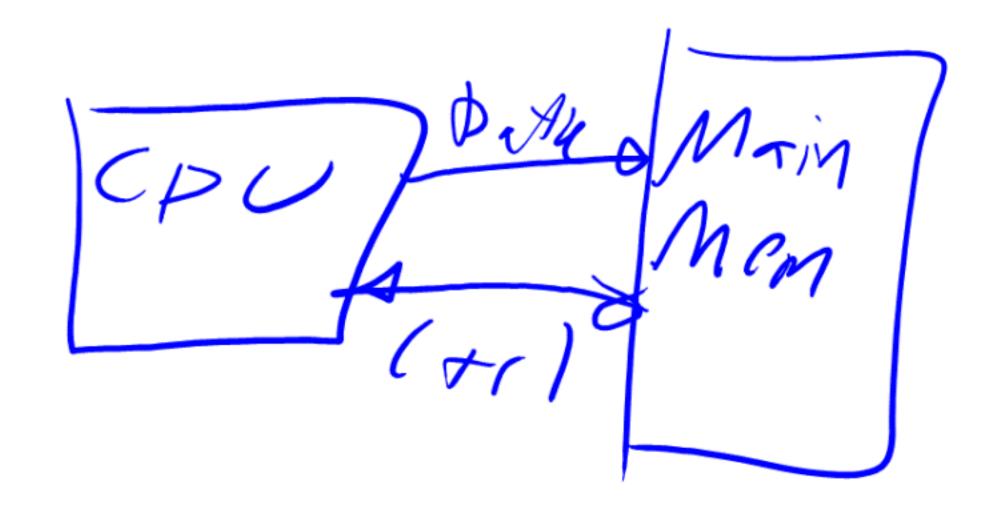
Lecture Objectives:

- Draw a picture of the on Neumann computer architecture
- Explain the concept of caching —
- 3) Define spatial locality and temporal locality
- List and define the categories of processing under Flynn's taxonomy





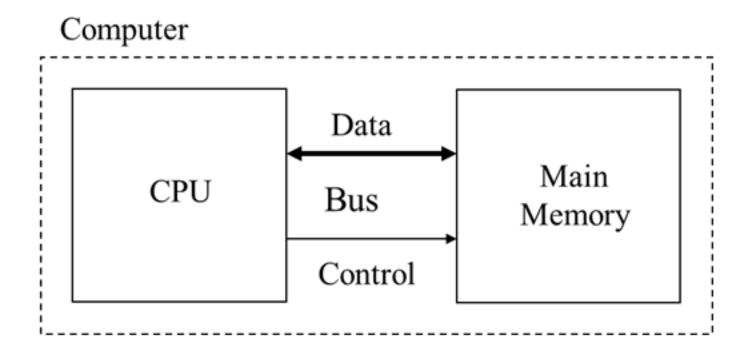






Principles

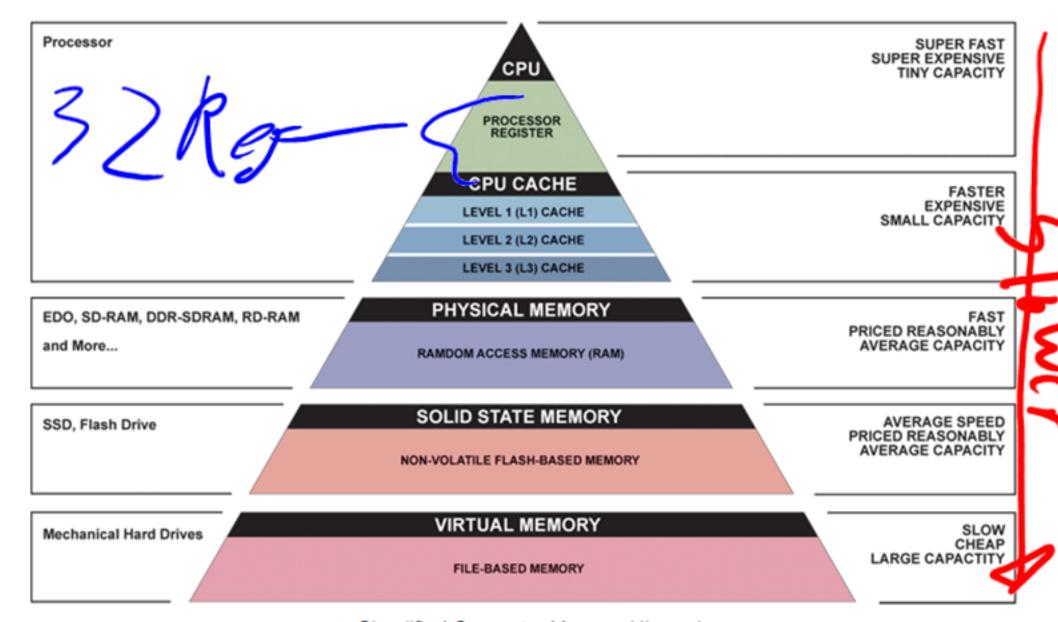
- Data and instructions are both stored in the main memory(stored program concept)
- The content of the memory is addressable by location (without regard to what is stored in that location)
- Instructions are executed sequentially unless the order is explicitly modified
- The basic architecture of the computer consists of:





How do we improve this





▲ Simplified Computer Memory Hierarchy Illustration: Ryan J. Leng





n the grocery store

- Tomatoes
- 2. Corn
- 3. Beans
- 4. Carrots
- 5. Bread
- 6. Peanut Butter
- 7. Cherry Jelly
- 8. Fresh Chicken Breas s
- 9. Rib Eye steaks 🖊
- 10. Spaghetti Sauce
- 11. Pasta Noodles
- 12. Milk
- 13. Yogurt
- 14. Mozzarella Cheese
- 15. Ice Cream
- 16. Cherry Lemon Sherbet

- Cherry Jelly
- 2. Corn
- 3. Ice Cream
- 4. Rib Eye Steaks
- Beans
- 6. Mozzarella Cheese
- Carrots
- 8. Bread
- 9. Fresh Chicken Breasts
- 10. Spaghetti Sauce
- 11. Milk
- Tomatoes
- 13. Peanut Butter
- 14. Yogurt
- 15. Pasta Noodles
- 16. Cherry Lemon Sherbet





Lets assume you coulc of time. change

| | _ | | | |
|----|-----|------|--------------|----|
| 1 | Ior | ทวเ | $r \sim c$ | 20 |
| Ι. | ıvı | ı ıa | \mathbf{L} | 53 |

- 2. Corn
- 3. Beans
- Carrots
- 5. Bread
- 6. Peanut Butter
- 7. Cherry Jelly
- Fresh Chicken Breasts
- Rib Eye steaks
- 10. Spaghetti Sauce
- 11. Pasta Noodles
- 12. Milk
- 13. Yogurt
- 14. Mozzarella Cheese
- 15. Ice Cream
- Cherry Lemon Sherbet





obtain anything from th Lets assume you could aisles . aisle change

- Cherry Jelly
- 2. Corn
- Ice Cream
- 4. Rib Eye Steaks
- 5. Beans
- 6. Mozzarella Cheese
- 7. Carrots
- Bread
- 9. Fresh Chicken Breasts
- Spaghetti Sauce
- 11. Milk__
- 12. Tomatoes
- 13. Peanut Butter
- 14. Yogurt
- 15. Pasta Noodles
- 16. Cherry Lemon Sherbet





Temporal Locality

 The principle stating that if a data location is referenced then it will again be referenced soon.

Spatial Locality

 The locality principle stating that if a data location is referenced, data locations with nearby addresses will tend to be referenced soon.





ets assume now that you go faster?

- 1. Tomatoes
- 2. Corn
- 3. Beans
- 4. Carrots
- 5. Bread
- 6. Peanut Butter
- 7. Cherry Jelly
- 8. Fresh Chicken Breasts
- 9. Rib Eye steaks
- 10. Spaghetti Sauce
- Pasta Noodles
- 12. Milk
- 13. Yogurt
- 14. Mozzarella Cheese
- 15. Ice Cream
- 16. Cherry Lemon Sherbet





- Attempts to improve processor performance by having multiple processor components (or functional units) simultaneously executing instructions
 - Pipelining

Multiple issue

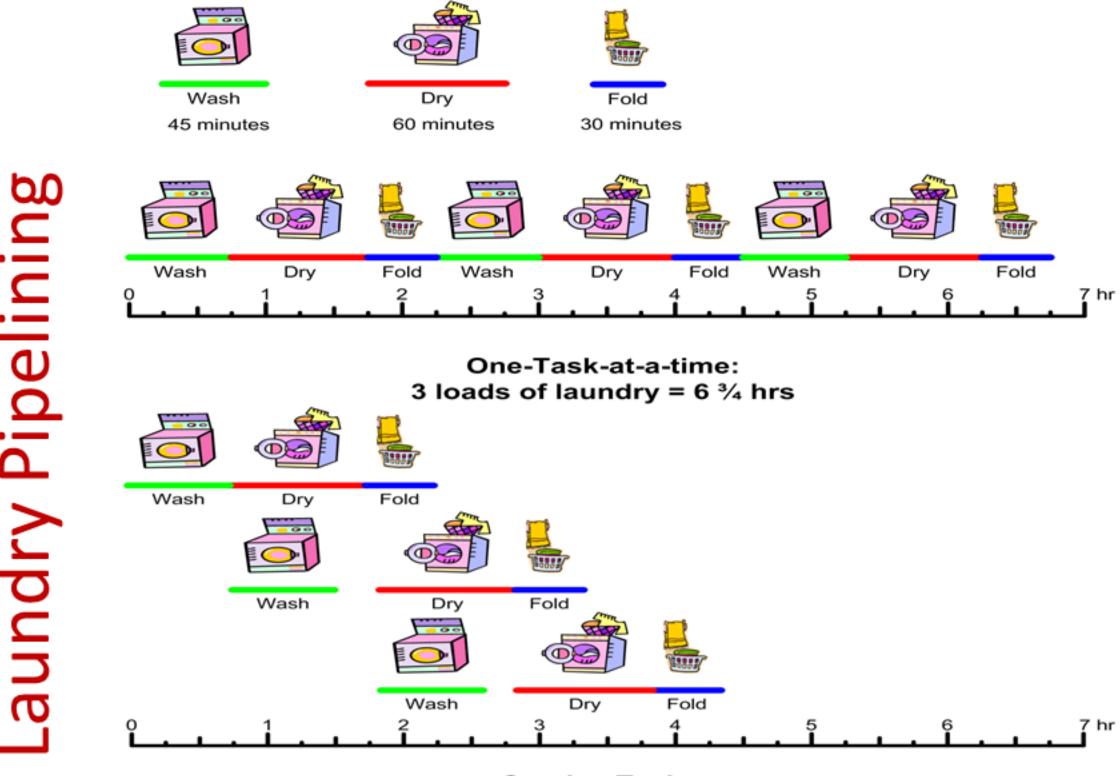


 Lets assume we are sending out a mass mailing by US Postal service and we have multiple people helping. How could we organize the process?

- Steps

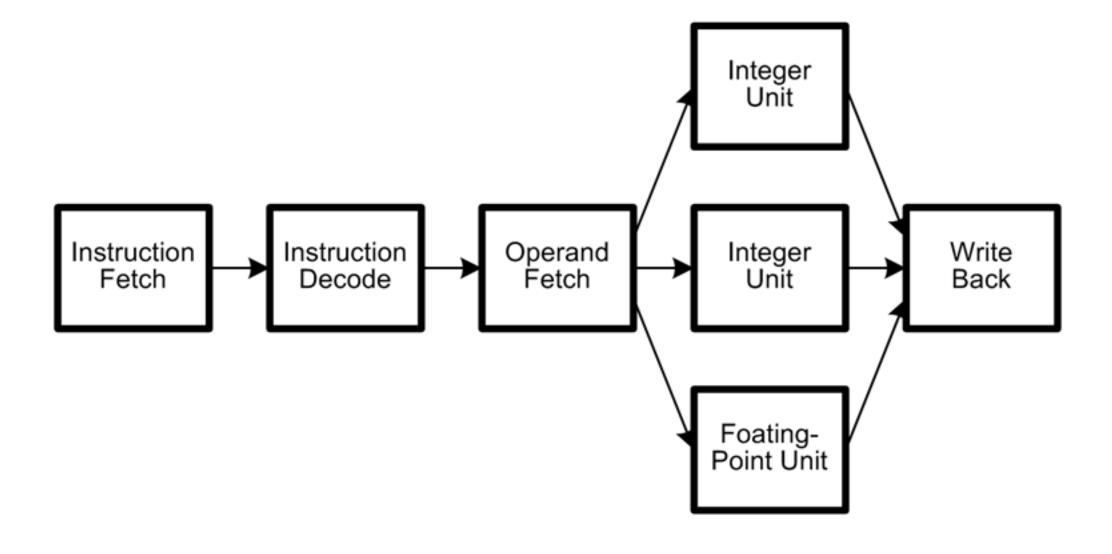






Overlap Tasks: 3 loads of laundry = 4 1/4 hrs







- Replicate functional units and attempt to execute different instructions in a program in tandem
- Example

 for (int index = 0; index < 1000; index++)

 {

 sum[index] = x[index]+y[index];

 for (index+1) = x(index)+y[index];



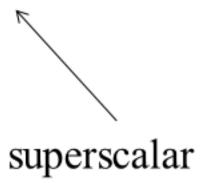
- Replicate functional units and attempt to execute different instructions in a program in tandem
- Example

```
for (int index = 0; index < 1000; index+=2)
{
  sum[index] = x[index]+y[index];
  sum[index+1] = x[index+1]+y[index+1];
}</pre>
```



 static multiple issue - functional units are scheduled at compile time.

 dynamic multiple issue – functional units are scheduled at run-time.





Static

 Multiple issue functional units are scheduled at compile time by the compiler

Dynamic

 Multiple issue functional units are scheduled at run-time



SISD

 Single Instruction, Single Data. This is the traditional single processor computer.

SIMD

Single Instruction, Multiple Data. This scheme, where a single instruction stream is executed by multiple ALUs

MISD

Multiple Instruction, Single Data.

MIMD

 Multiple Instruction, Multiple Data. This is currently The most popular hardware design for parallel processors.



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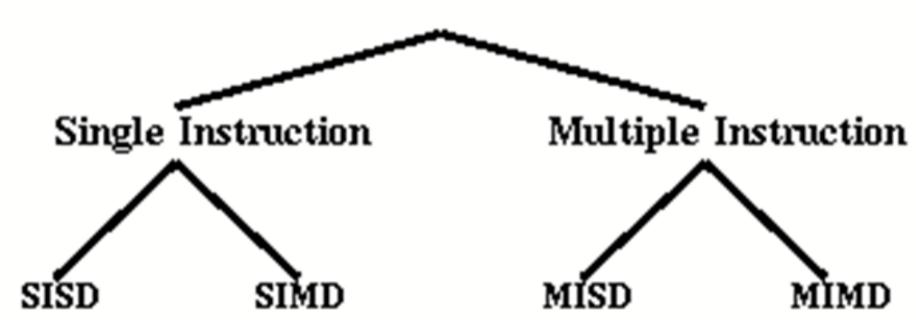
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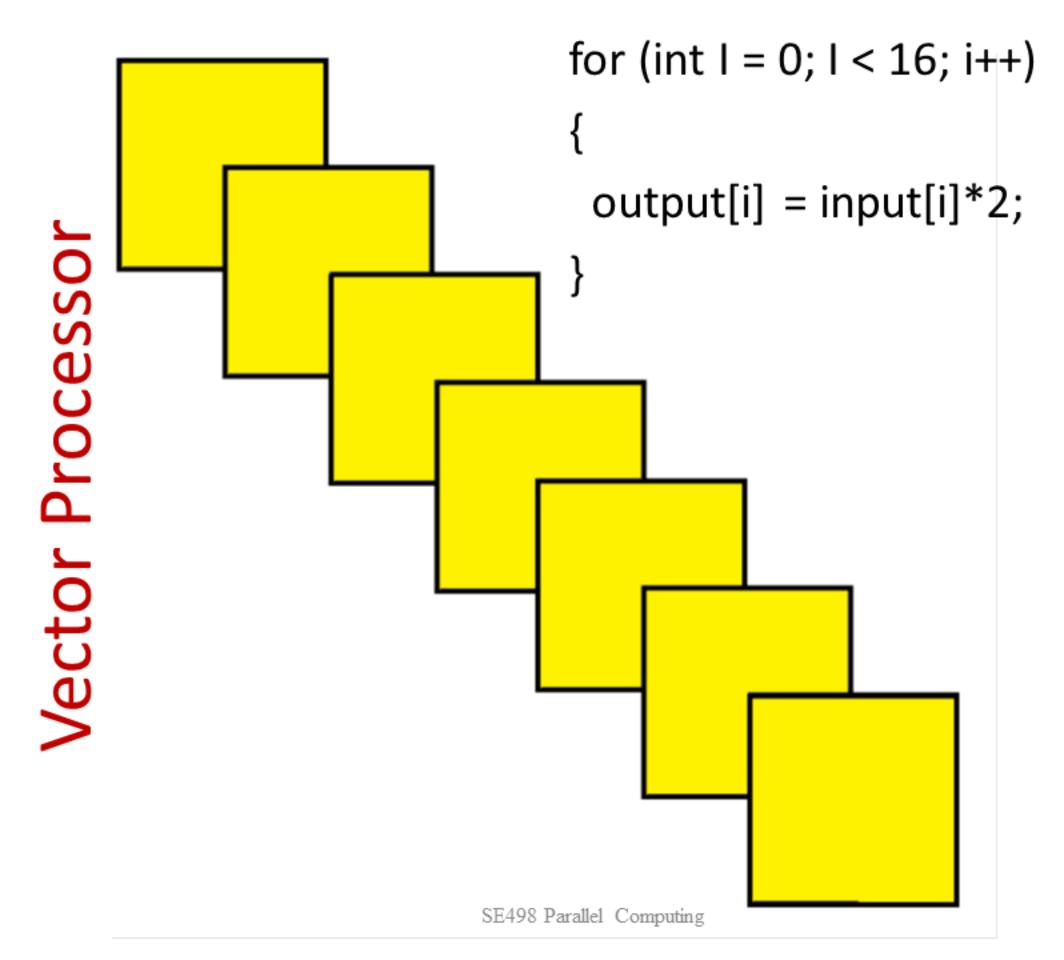
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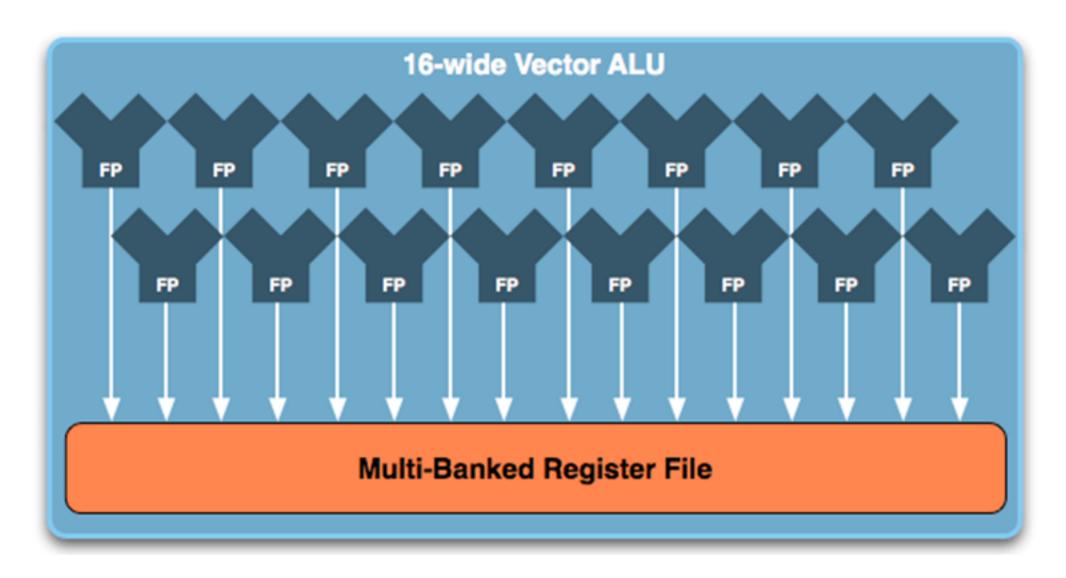








structure



*http://www.anandtech.com/show/6017/intel-announts xeon-phi-family-of-coprocessors-mic-goes-retail

