Parallel Hardware
Part 2

Lecture Objectives:

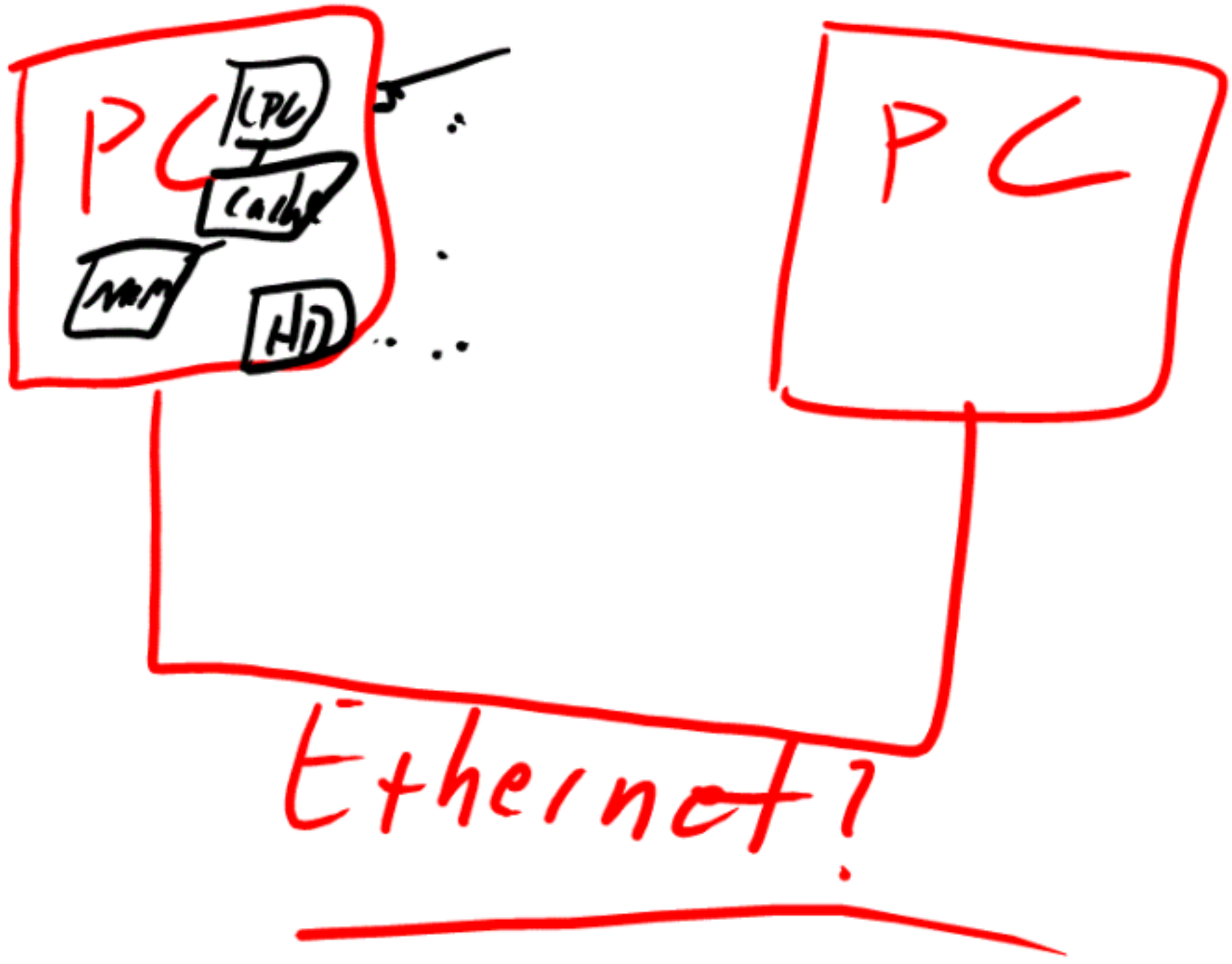
1) Compare and contrast a shared memory system with a distributed memory system from an architectural standpoint
2) Compare and contrast NORMA, NUMA, and UMA multicore systems
3) Draw a picture of a switched interconnect topology using a crossbar connection
4) Explain the concepts of a ring, a torroidal mesh, bisected ring, fully connected network, and hypercube architecture.
5) Define the terms latency and bandwidth, and explain the implication on parallel computing.

Reading Quiz Question

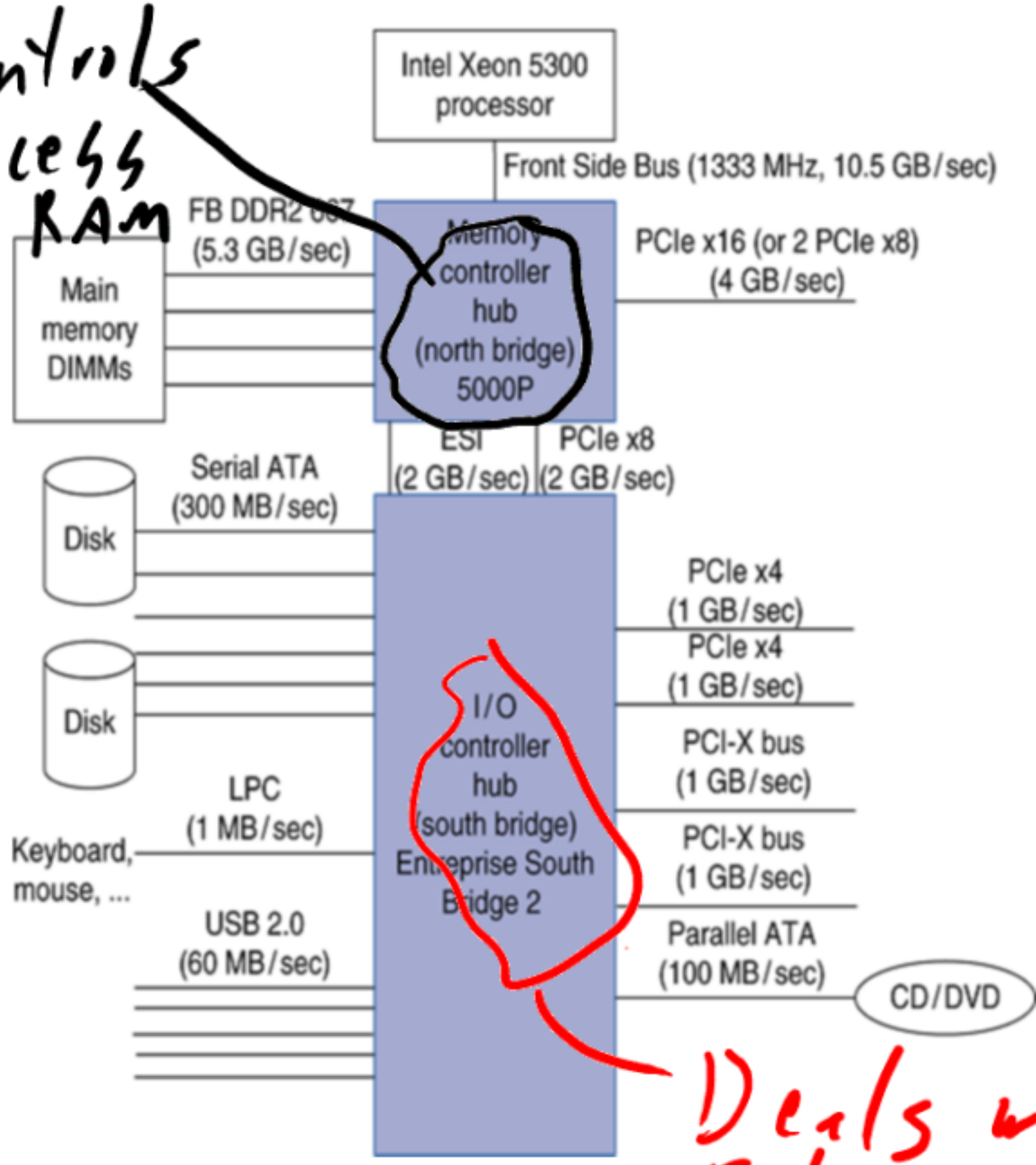
- What does MIMD stand for?

Multiple Instructions
Multiple Data

How would you connect multiple computers together?



A Basic Computer Design

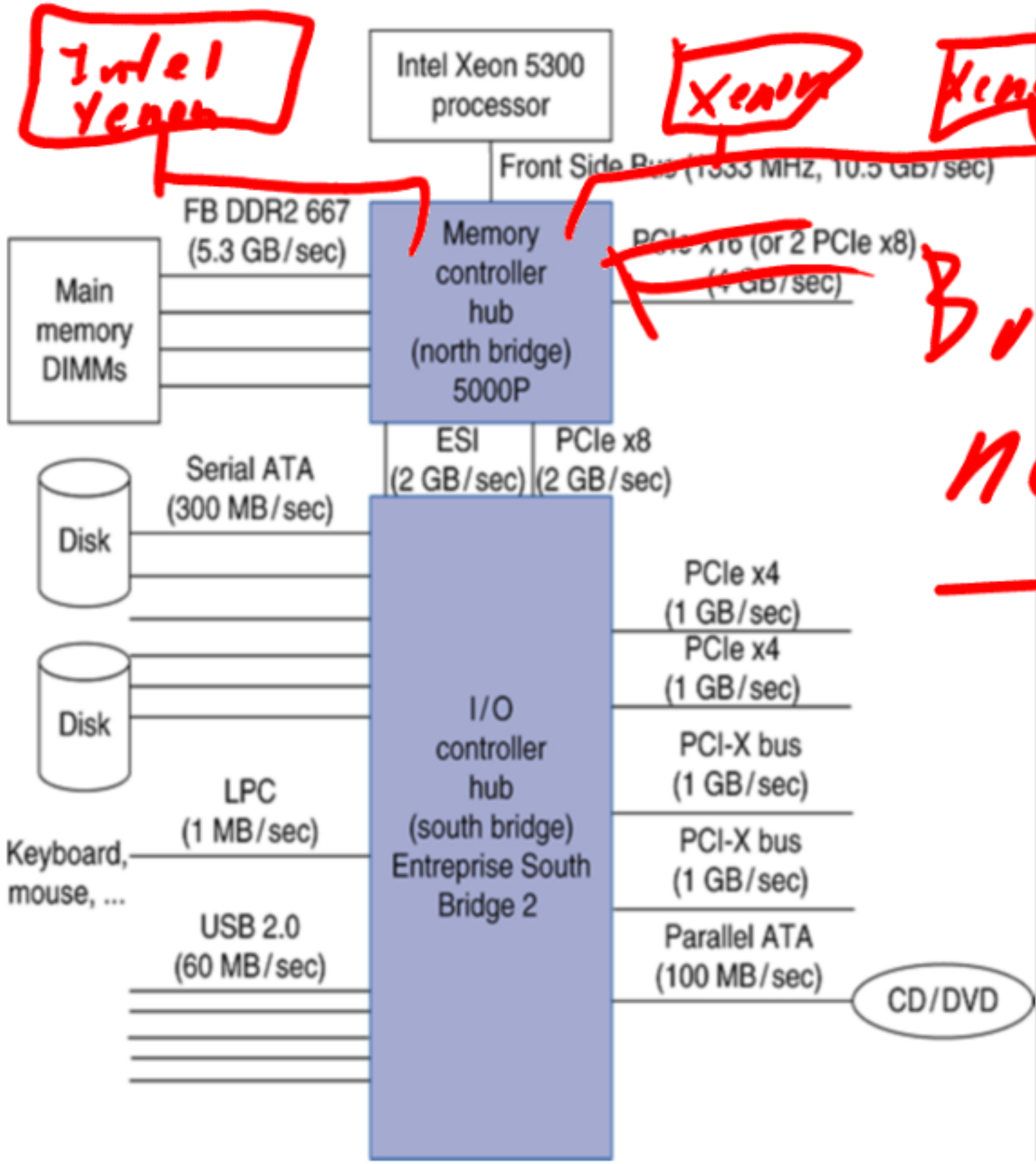


Controls access to RAM

Deals w/ external HW

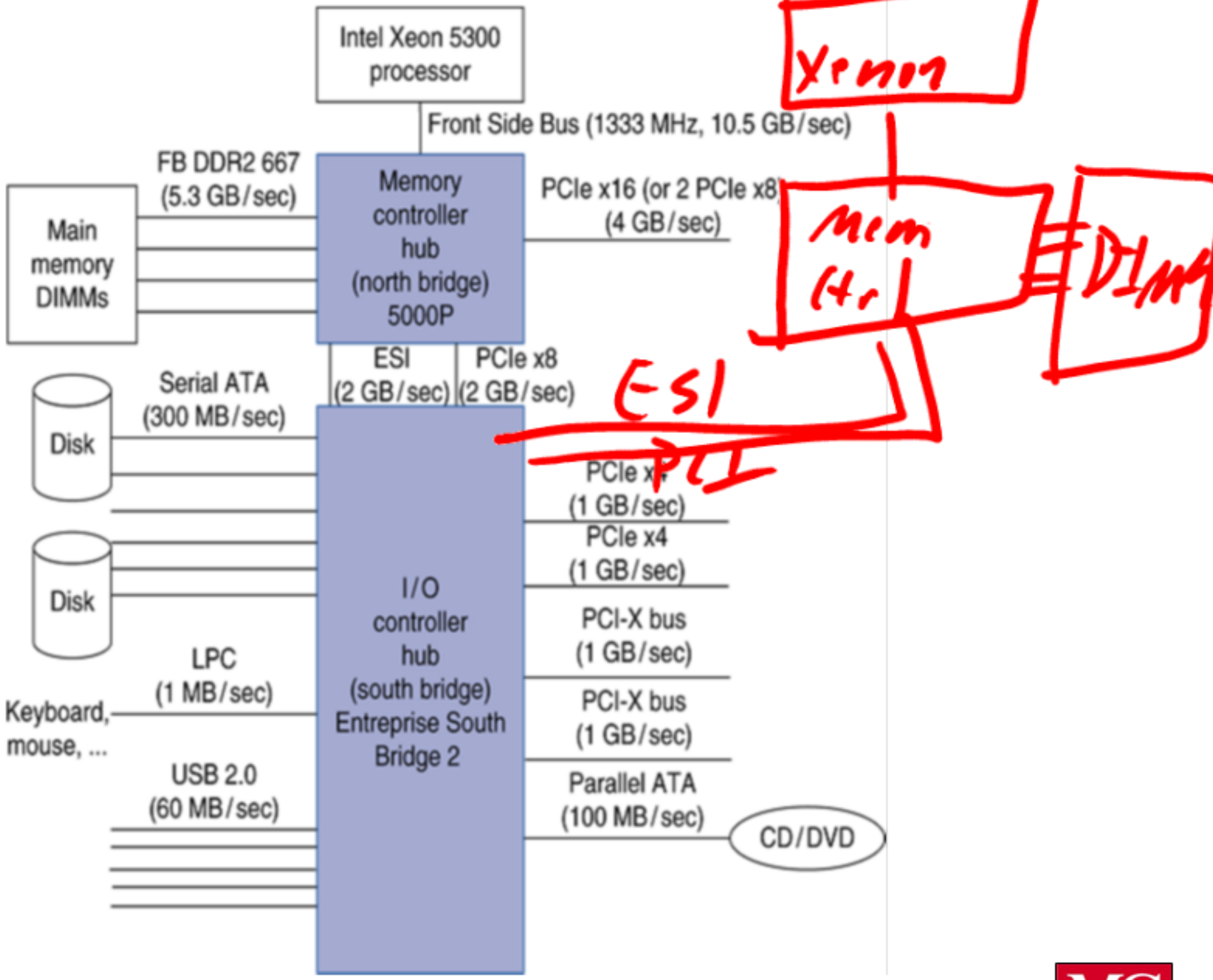
*Patterson and Hennessy: Computer Organization and Design

A Shared Memory System



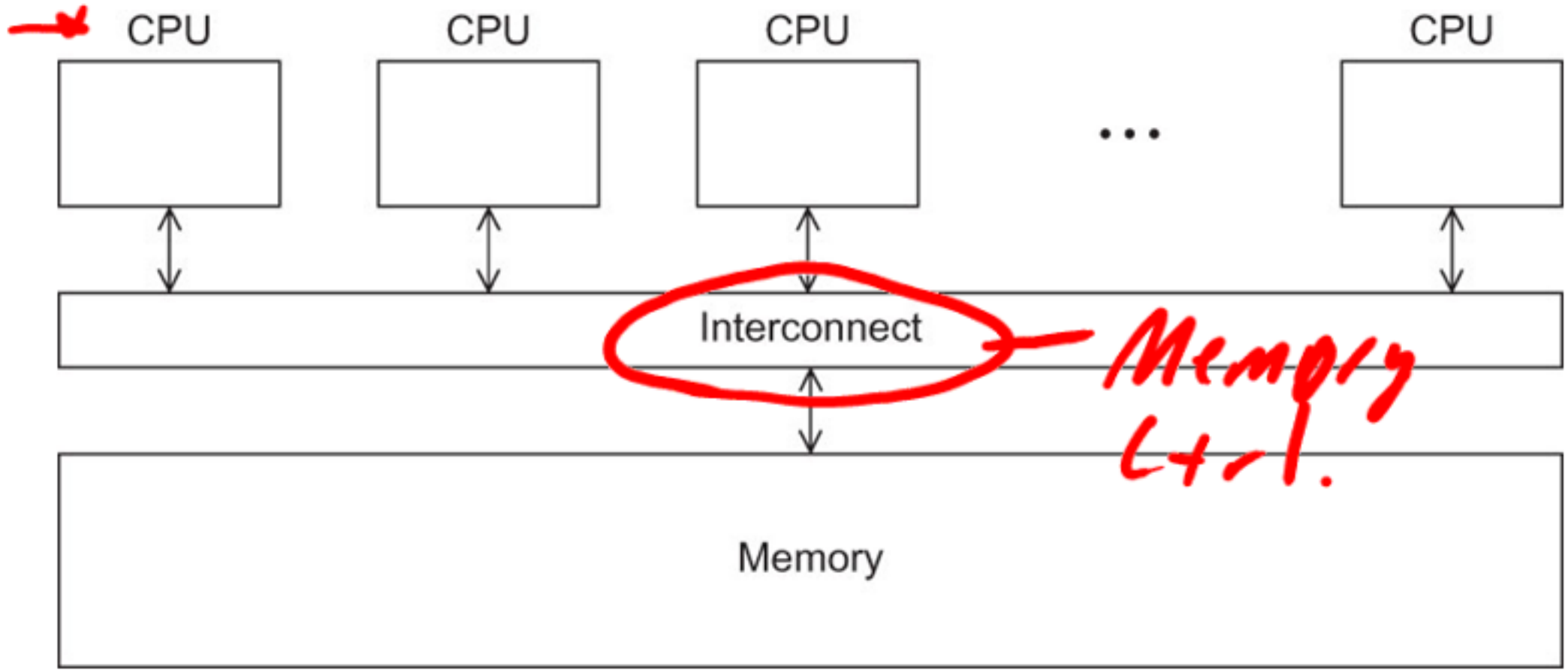
*Patterson and Hennessy: Computer Organization and Design

A Shared Memory System



*Patterson and Hennessy: Computer Organization and Design

A Refined Shared Memory System



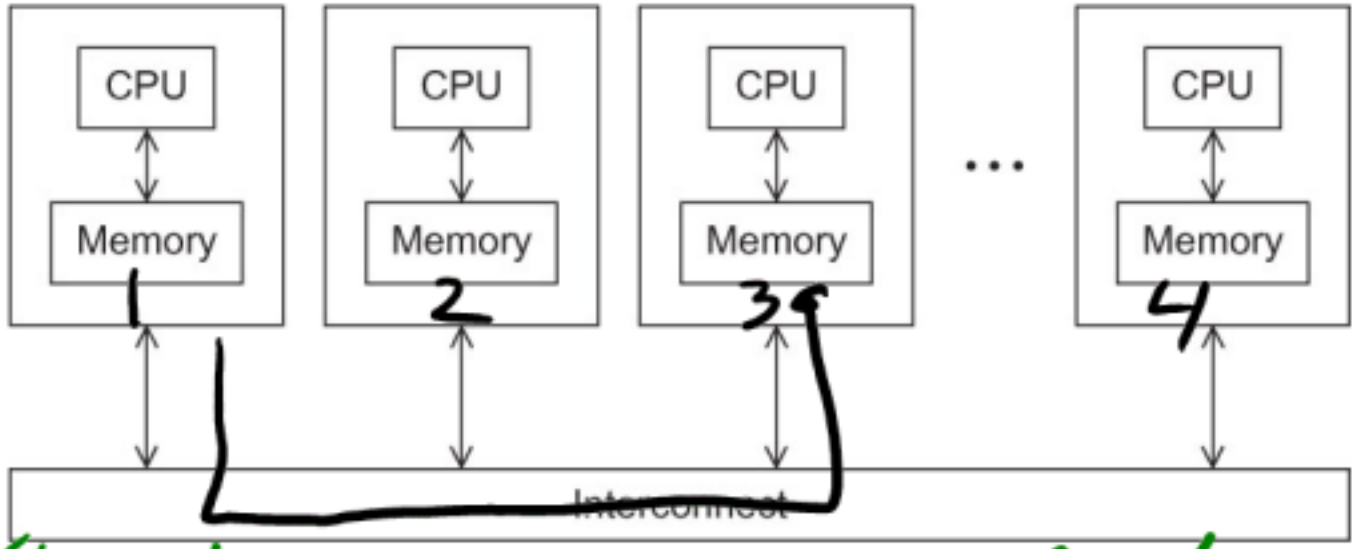
Each processor can access all system memory.

Challenge: Designing the interconnect.

Advantage: less overhead.

Disadvantage: Not as scalable. Hard to build for more than a few CPUs.

Distributed Memory System



Each processor is paired w/ some private memory.

Easier: To design + given core

Generally more scalable

MSOE

NUMA

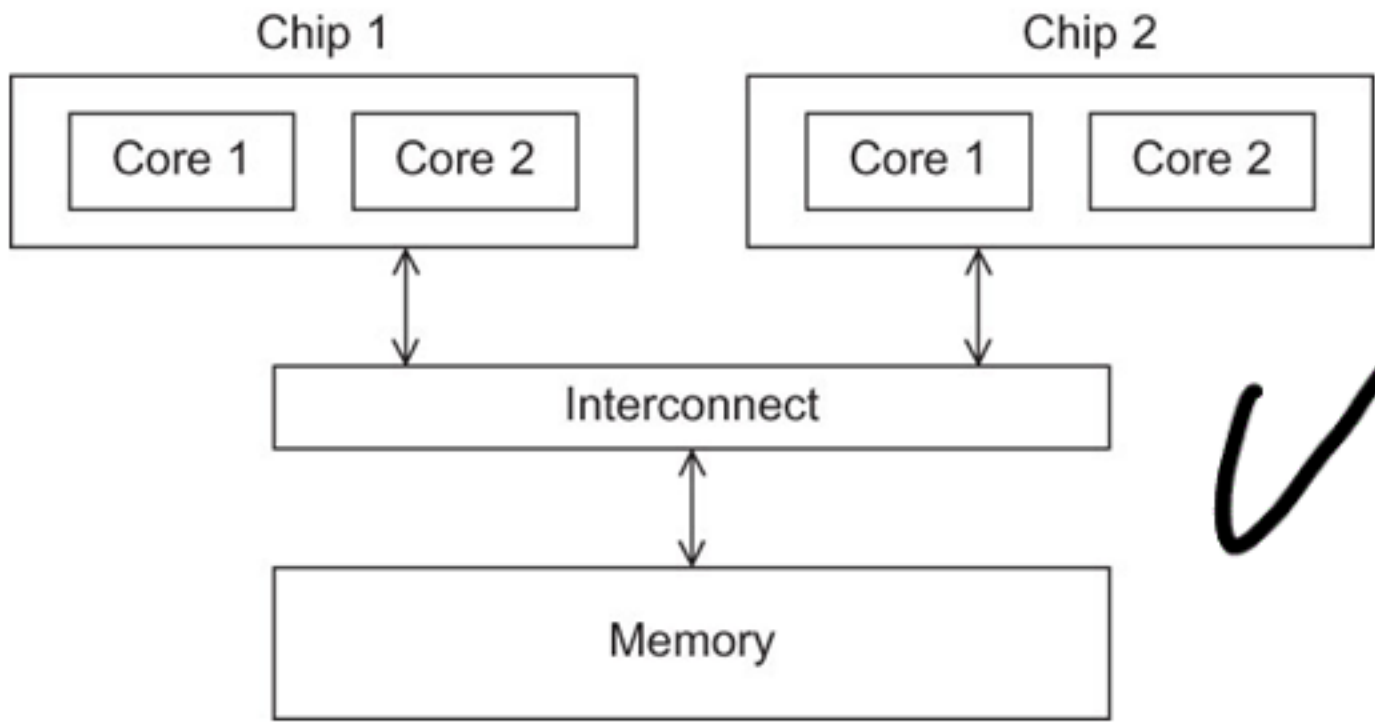
Harder to work w/ from a SW standpoint.

May be less performance

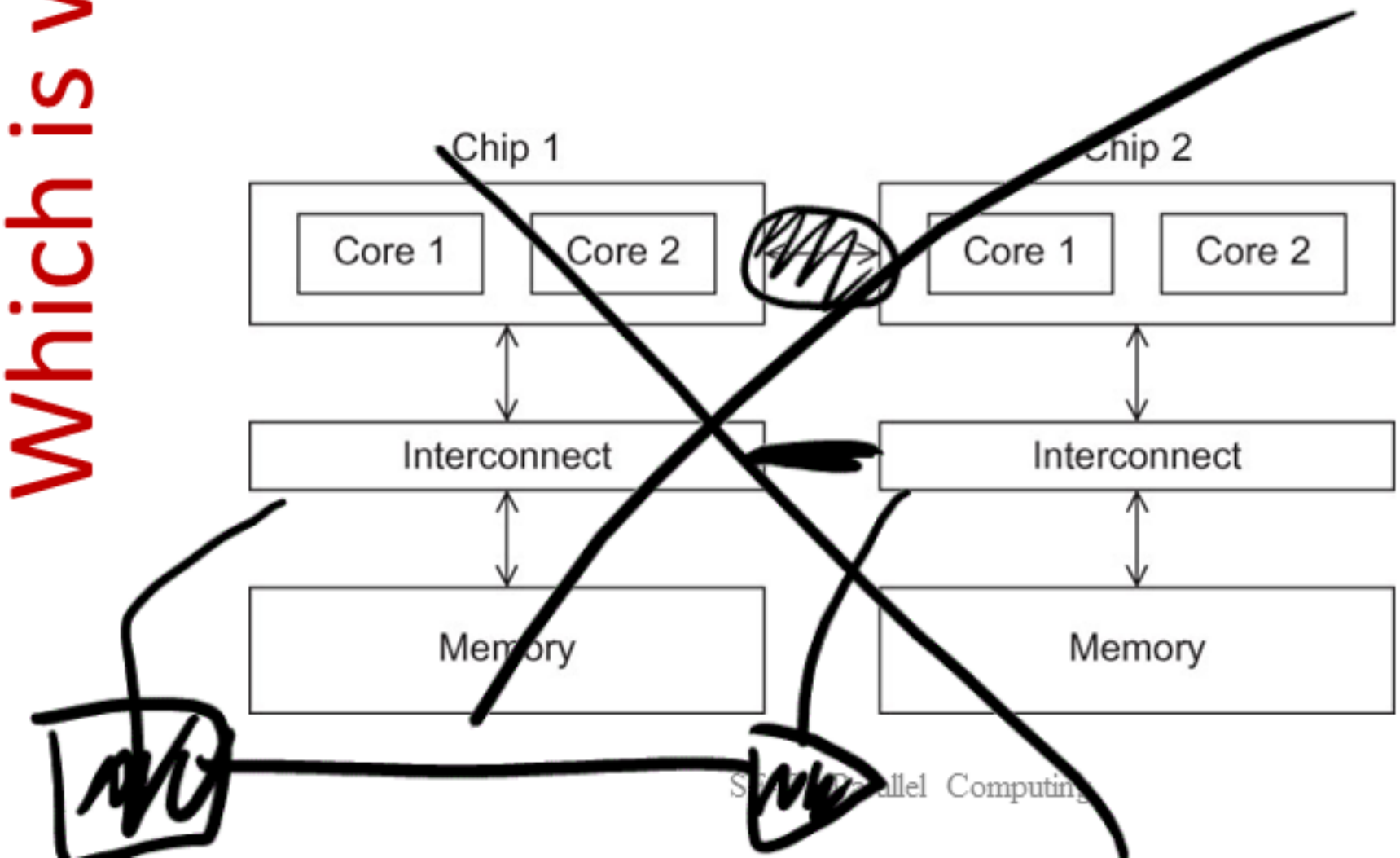
Definitions

- UMA
  - Uniform Memory Access
    - The access time to all memory is the same, regardless of the processor core's location.
- NUMA
  - Non-Uniform Memory Access
    - The access time is different depending on where in memory a piece of data is located
- NORMA
  - No Remote Memory Access
    - All memory needed from a remote machine must be requested using a message

Which is which?



UMA



Normal NUMA

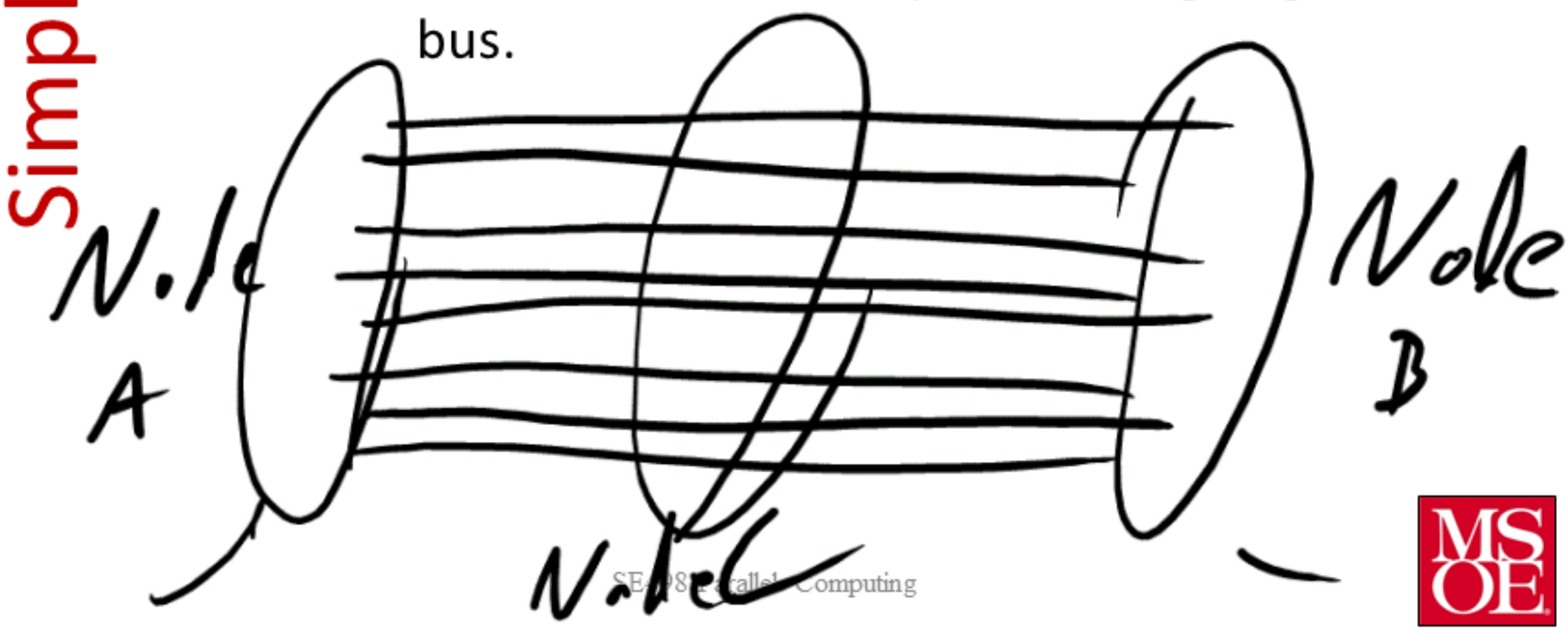
MSOE

Interconnection Networks

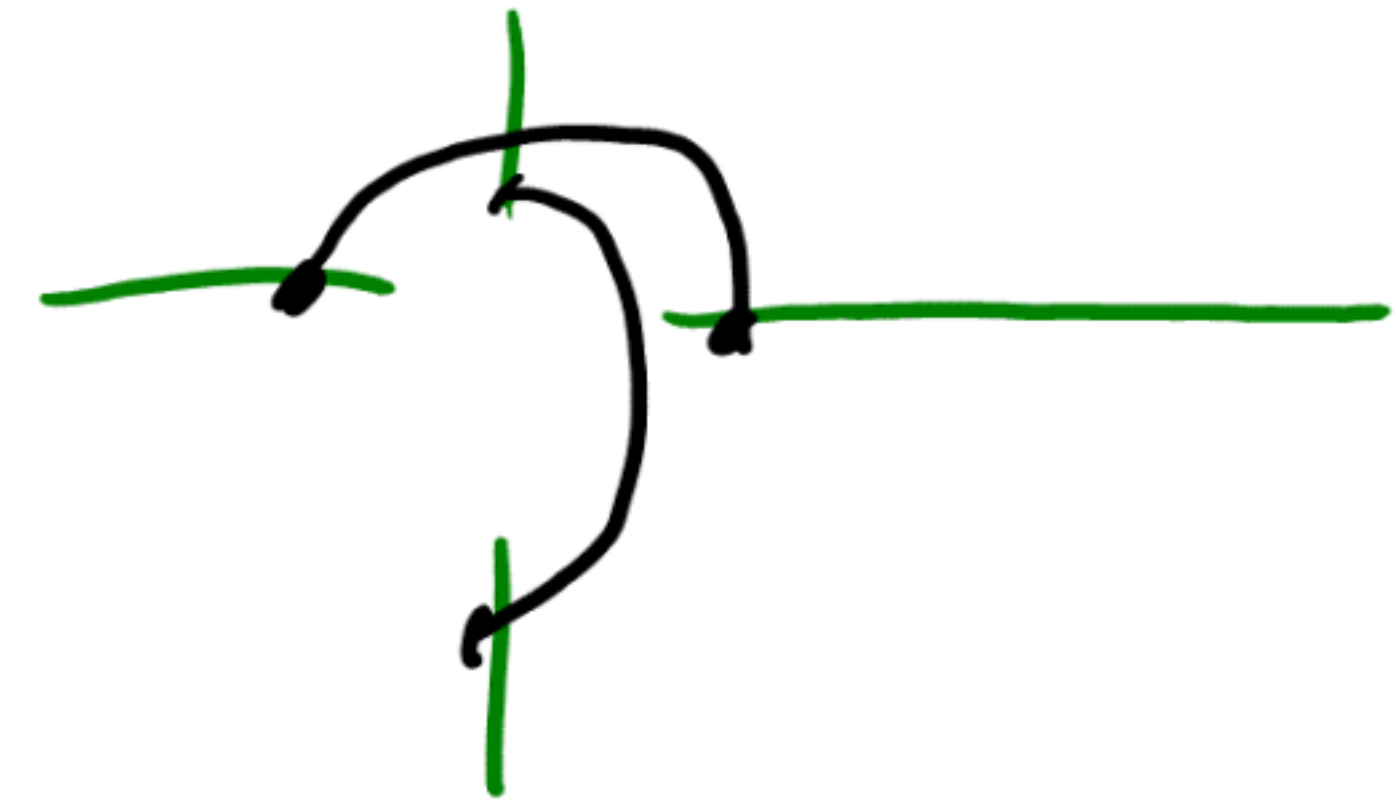
- Very important to have an appropriate interconnection network
  - Slow interconnect will degrade the performance of "perfect" processors

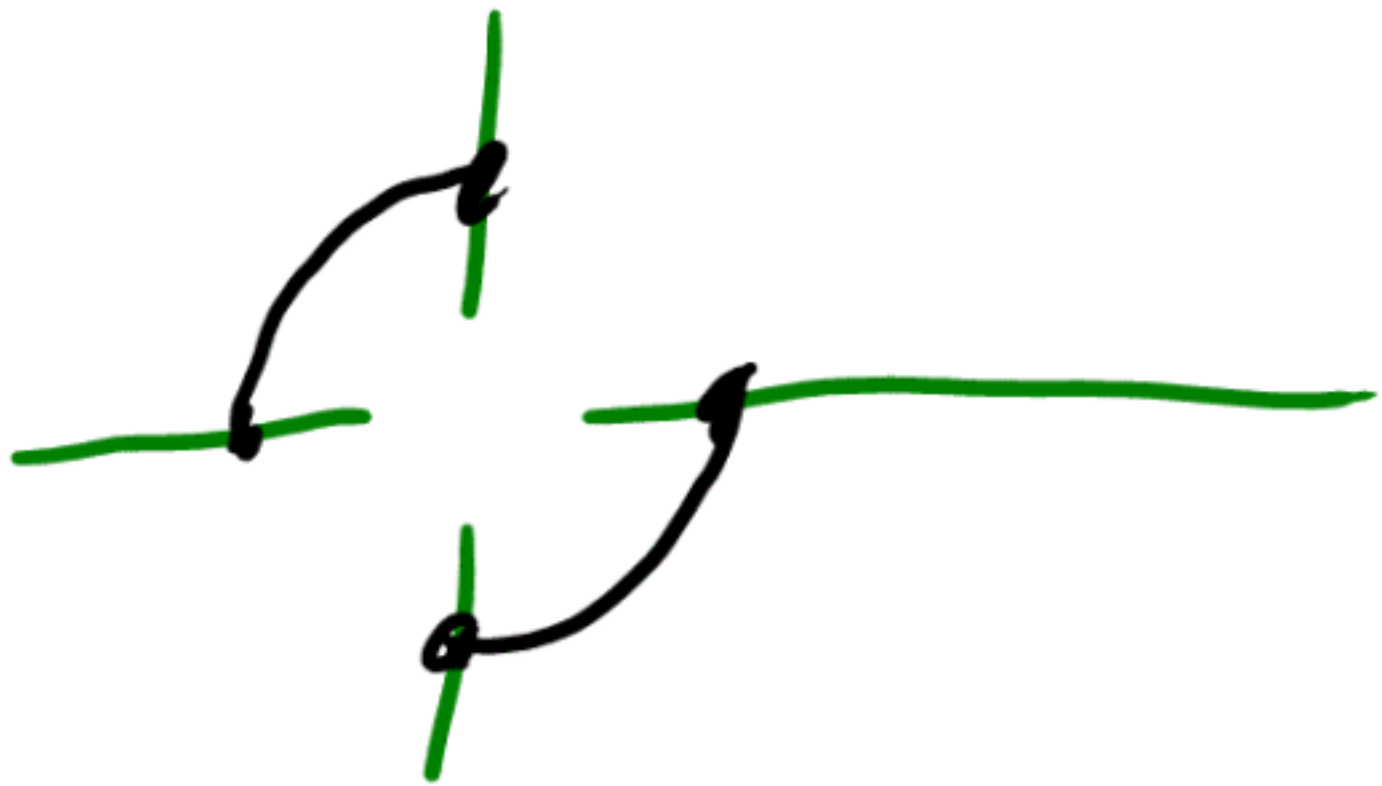
Simple Bus

- A set of parallel communication wires between devices
  - Wires are shared by all devices
  - Low cost
  - But
    - If a large number of processors are on the bus, a lot of time will be spent waiting to get the bus.

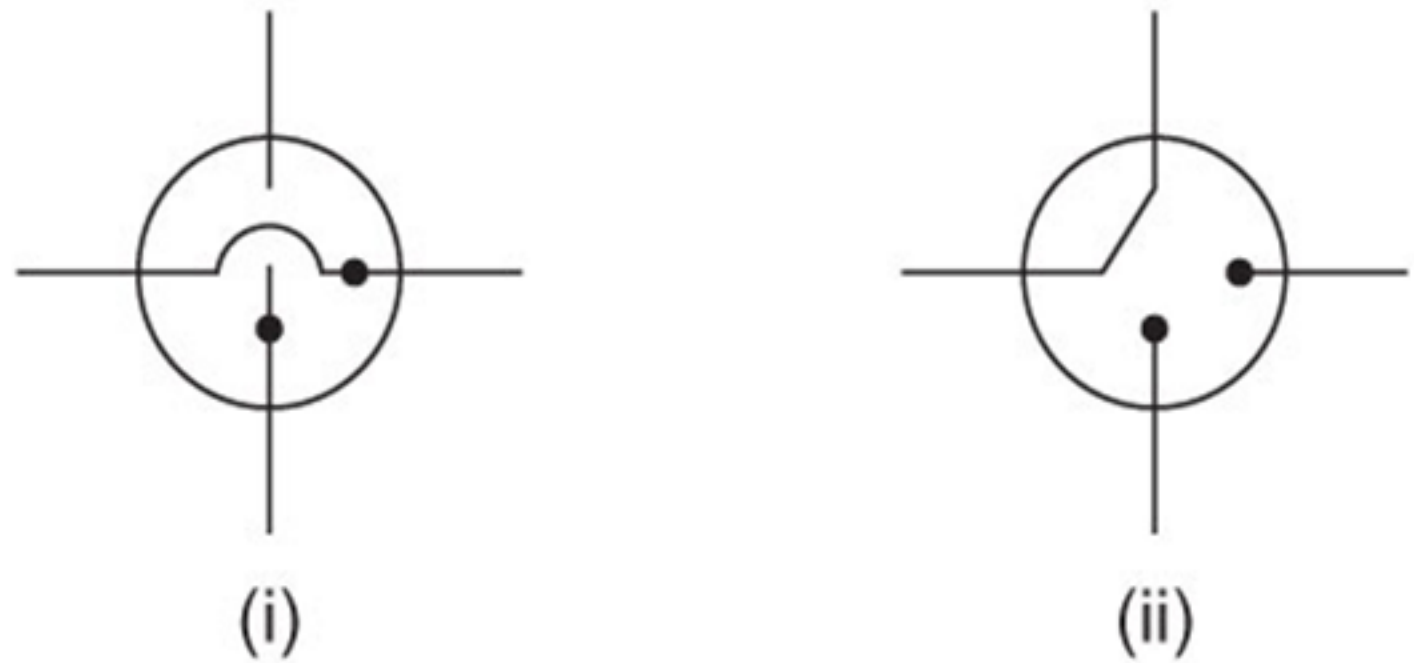


Switched interconnect (AKA Crossbar)



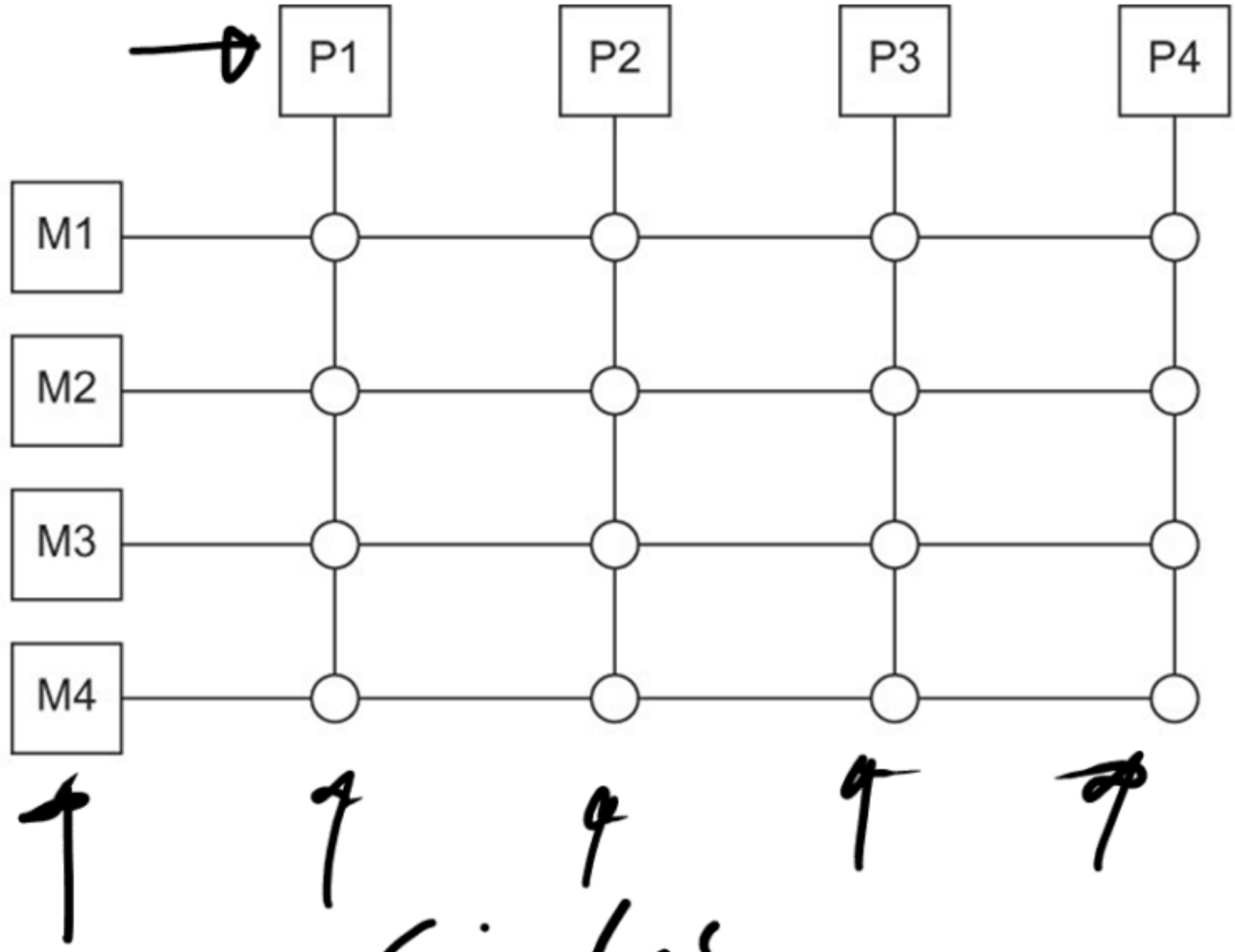


Switched interconnect - Switch



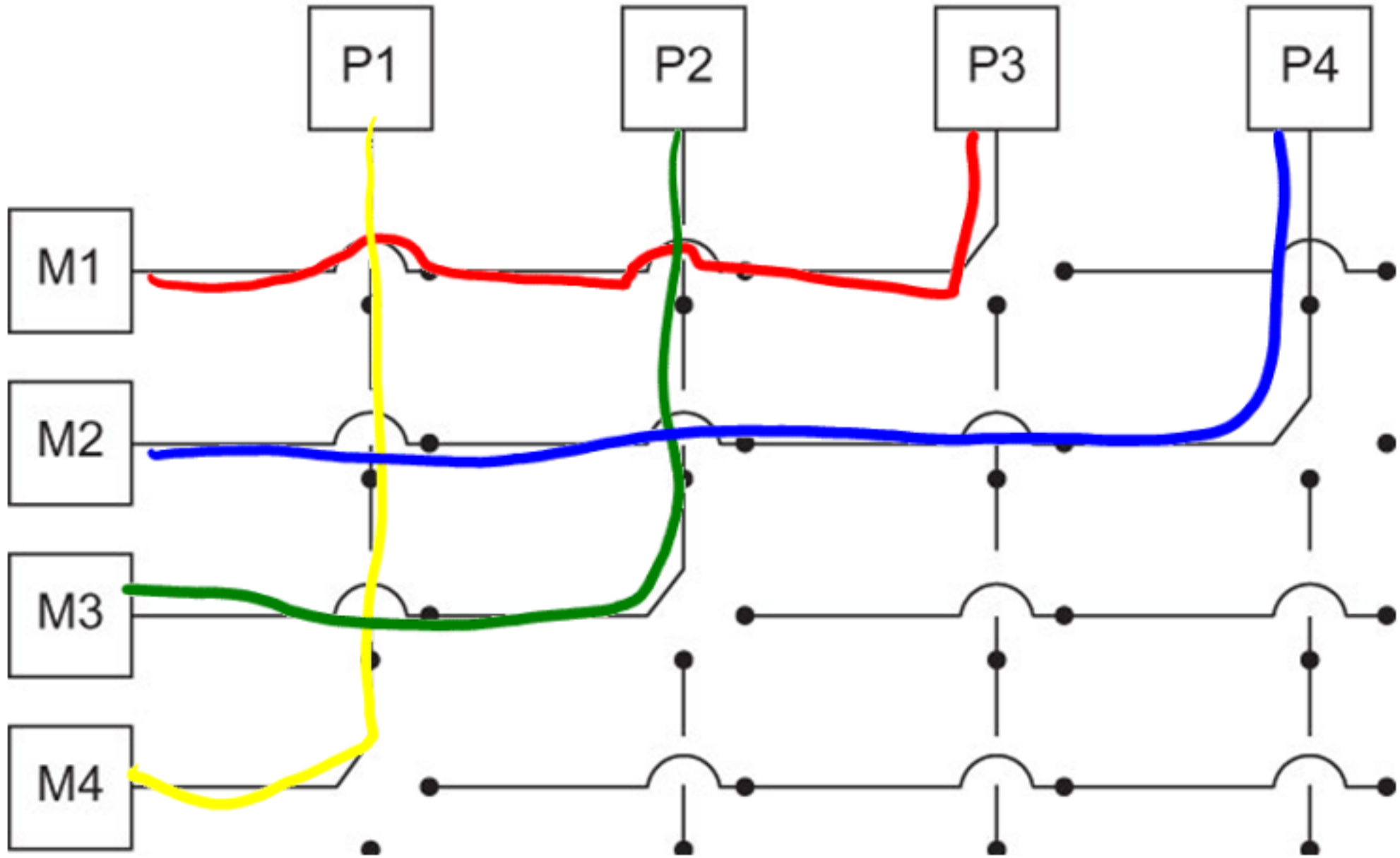
Switched interconnect - Layout

Switched interconnect - Layout



Switched interconnect - Connections

Switched interconnect - Connections



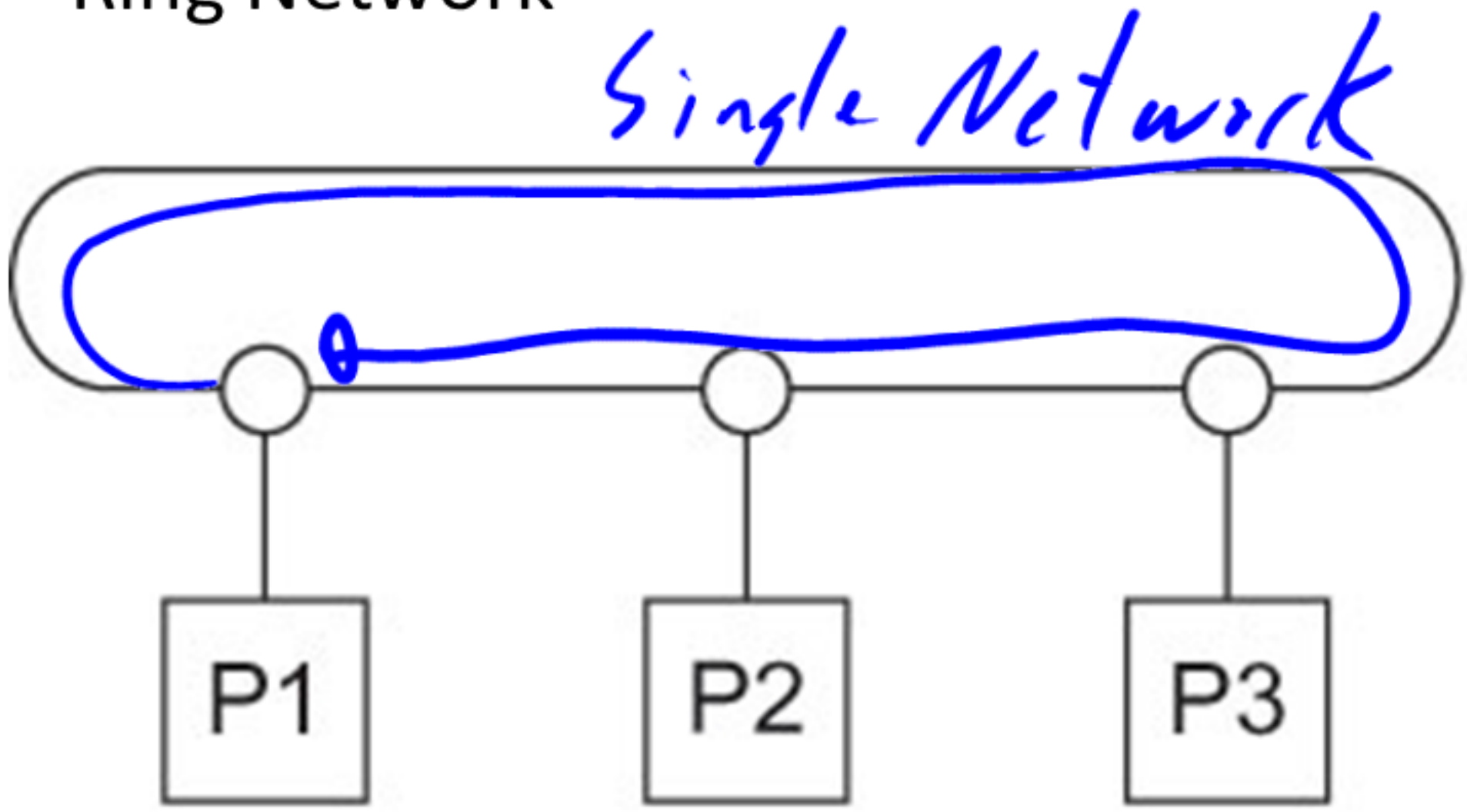
Crossbar Advantages / Disadvantages

- Advantages
  - Very high performance can be achieved
  - Simultaneous communication between devices is possible
- Disadvantage
  - Cost of switches is very high
  - Complex to design as systems get larger

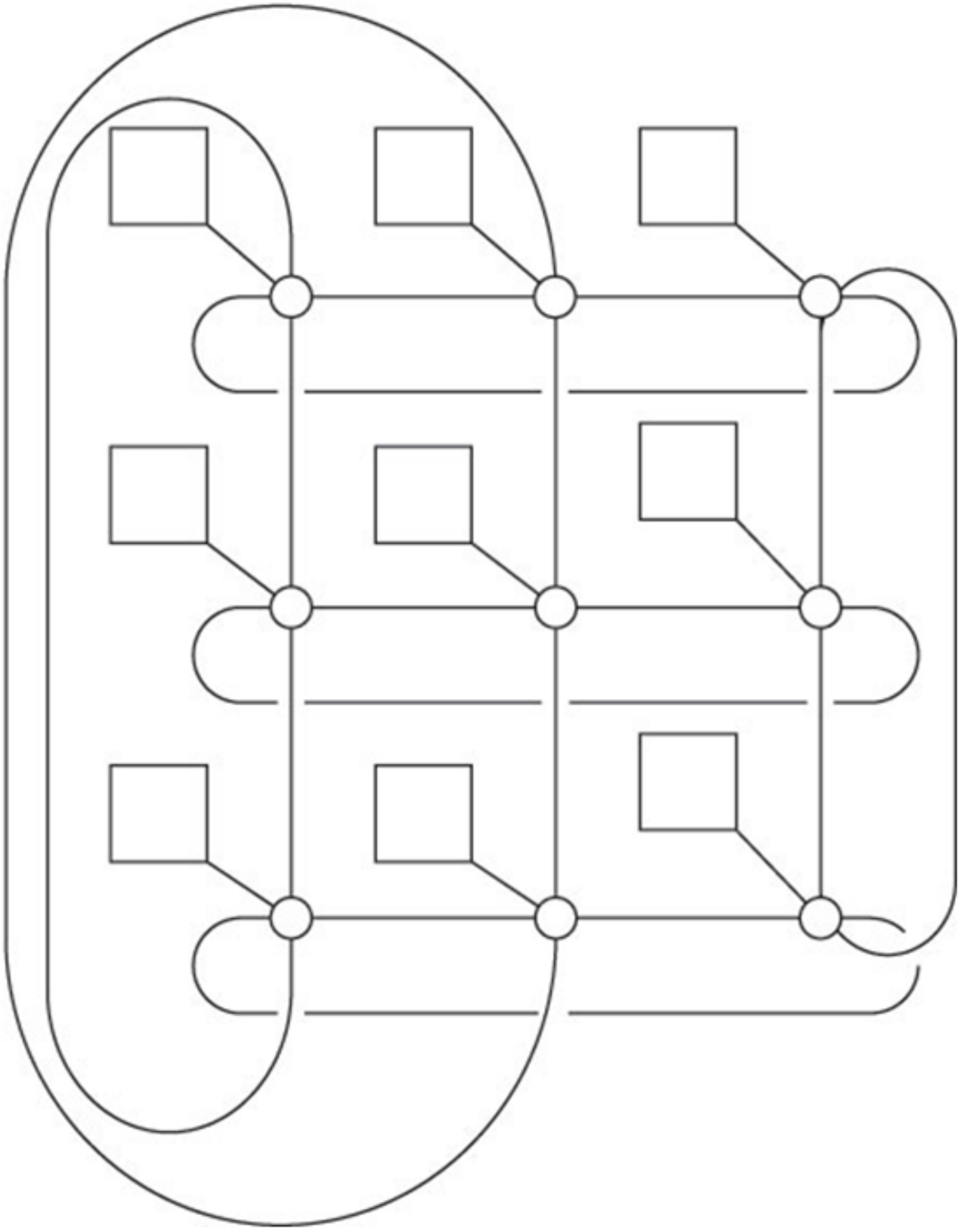
Connecting Distributed Systems

- Ring Network

- Ring Network



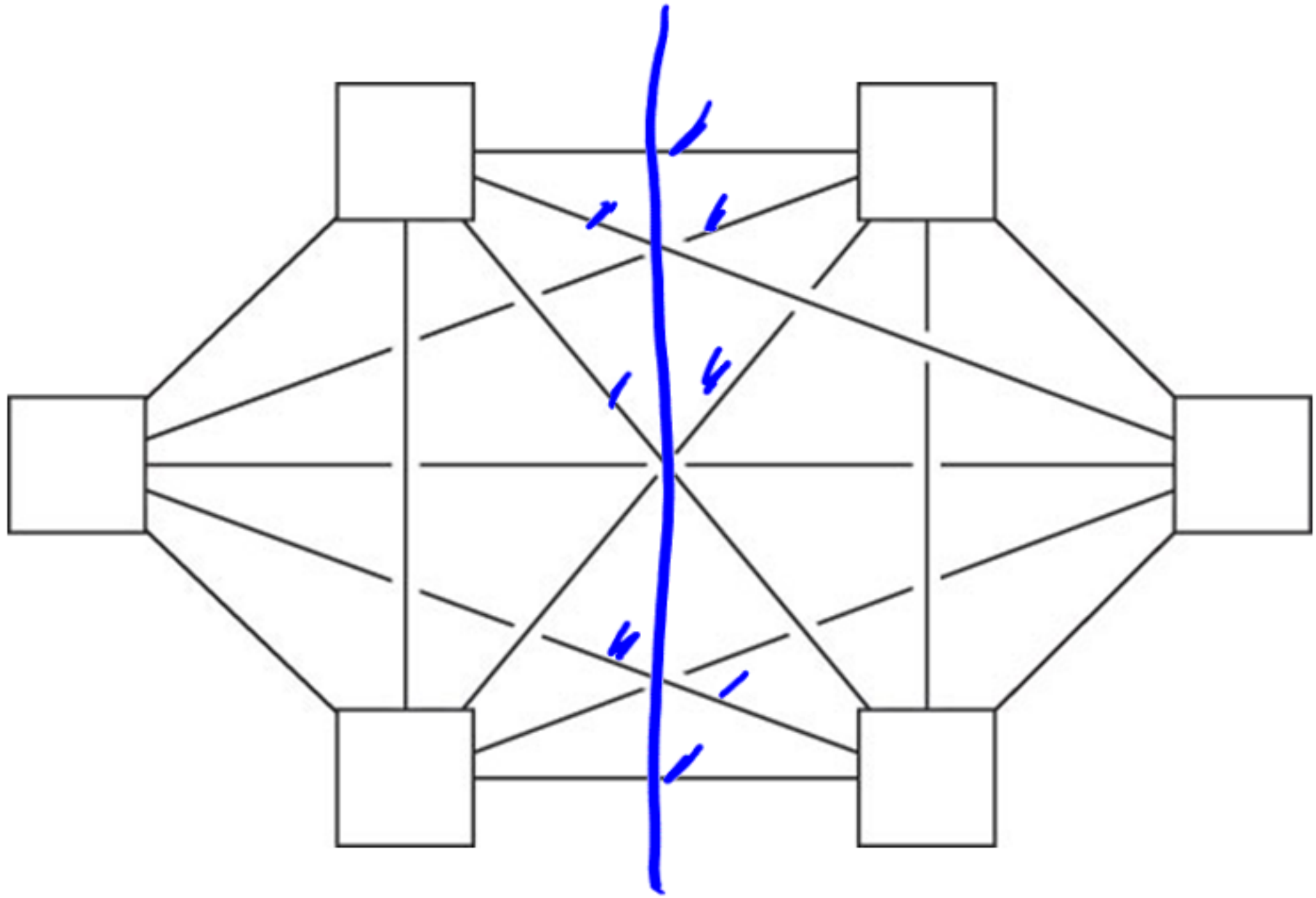
Connecting Distributed Memory Systems – Toroidal Mesh



Definitions

- Diameter
  - The diameter of a network is the largest distance between 2 nodes
- Bisection Width
  - The minimum number of edges that must be removed in order to divide the network into 2 halves
- Bisection Bandwidth
  - The sum of the bandwidth of the bisection width connections

Fully connected network

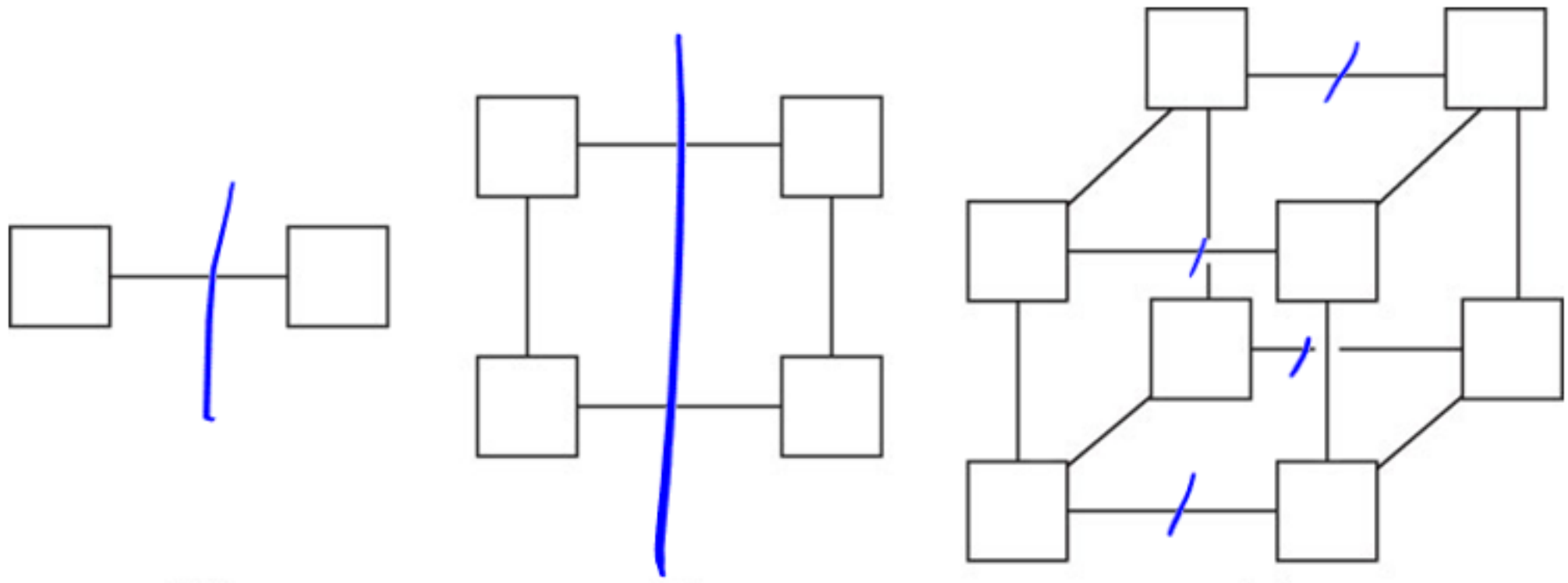


Diameter – 1

Bisection Bandwidth: 8 9

Bandwidth: 9 x BW.

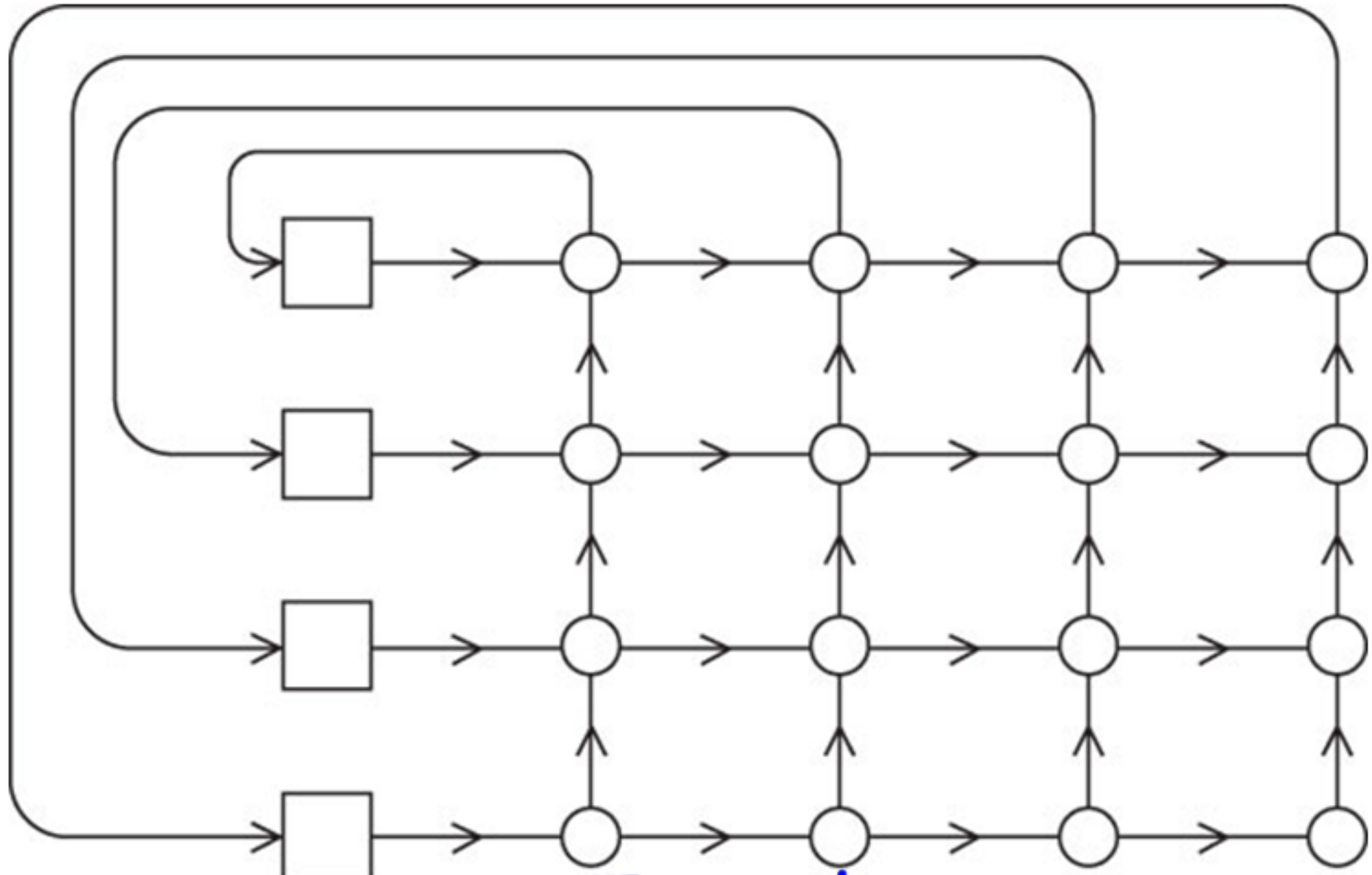
Hypercubes



Hypercube:
Diameter: # of dimensions
Bisection width: $\frac{1}{2}$ # of dimensions

MSOE

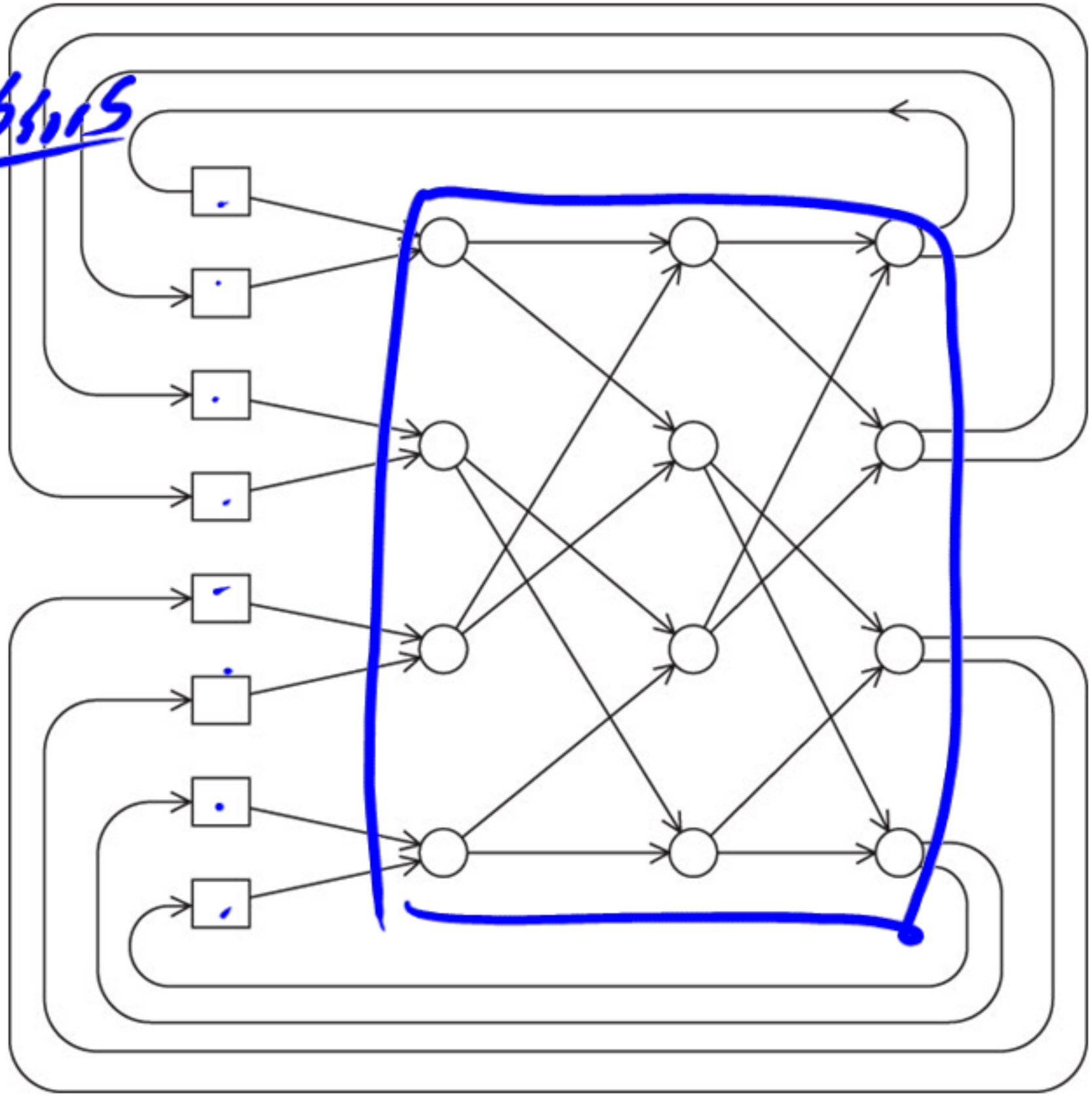
Crossbar Interconnect



MSOE

8 processors

Omega Network



Topology Summaries

Network	Nodes	Diameter	Bisection Width
1 D Mesh	K	k-1	1
2D Mesh	K^2	2(k-1)	K
3D Mesh	K^3	3(k-1)	K^2
Binary Tree	2k-1	2(k-1)	1
Pyramid	$(4k^2-1)/3$	2k	2k
Hypercube	2k	2k-1	2^{k-1}
Cube Connected Cycle Network	$k2^k$	2k	2^{k-1}

Latency and Bandwidth

- Latency
  - The time from the source sending the first byte until the destination receives the first byte of a message
    - L – given in seconds
- Bandwidth
  - The rate at which the destination receives data from the source
    - B – bytes per second

$$message\ Tx\ Time = l + \frac{n}{b}$$