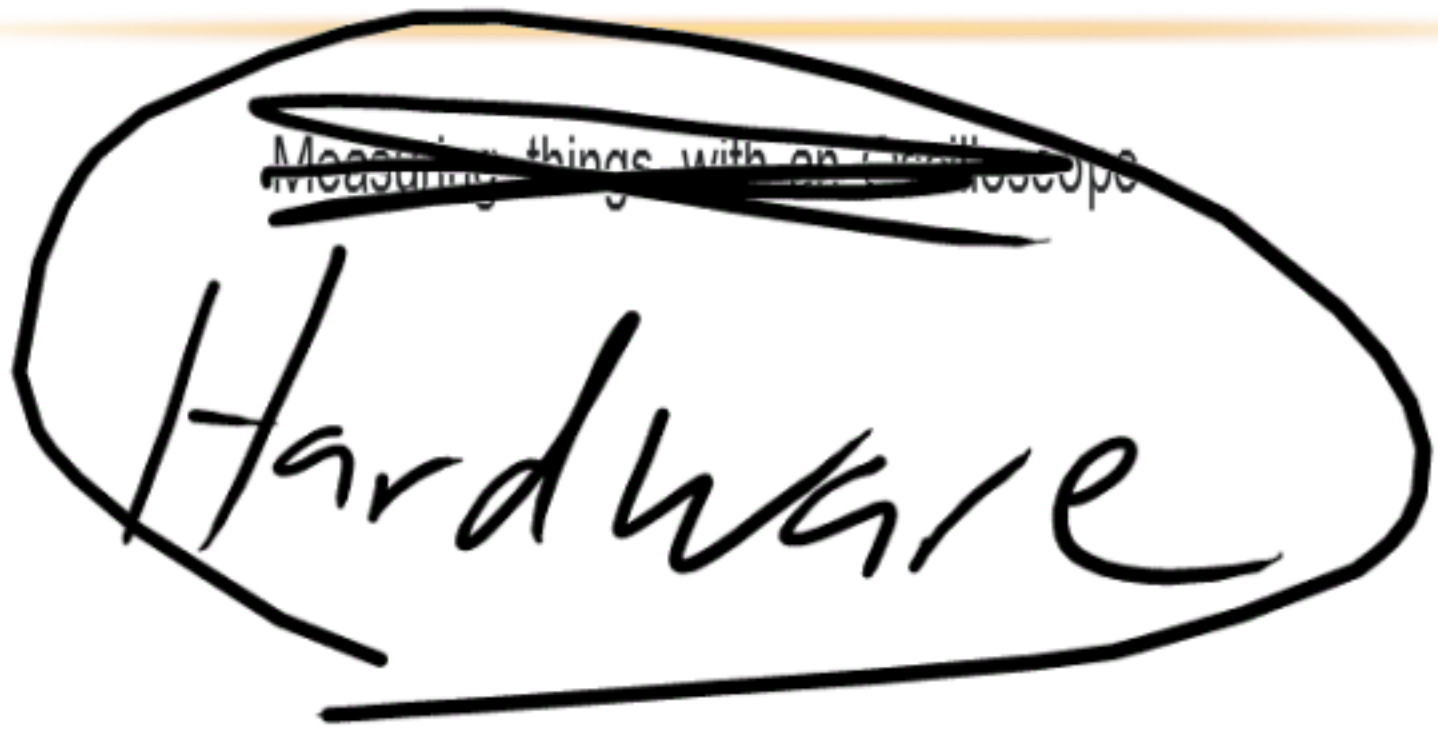
SE3910 – REAL TIME SYSTEMS



OBJECTIVES

- Explain the difference between a microcontroller and a microprocessor
- Identify the key components of the Beaglebone platform
- Explain why the Beaglebone changes operating frequency under different power conditions
- Identify the key hardware interfaces of the beaglebone
- Explain the concept of a cape
- Calculate the software GPIO pin number from an expansion port header definition
- Understand how to read a basic schematic
- Explain the concept of a dropping resistor
- Explain the concept of a pull up and a pull down resistor

POP QUIZ

- What is the key factor which defines a real time system versus a non real time system
  a. Fast I/O
  b. Small systems
  c. Deterministic response
  d. High speed operation
  e. Correctness only depends on logic

useless

POP QUIZ

- What is the key item which defines an embedded system versus a non-embedded system

a. Hardware only design

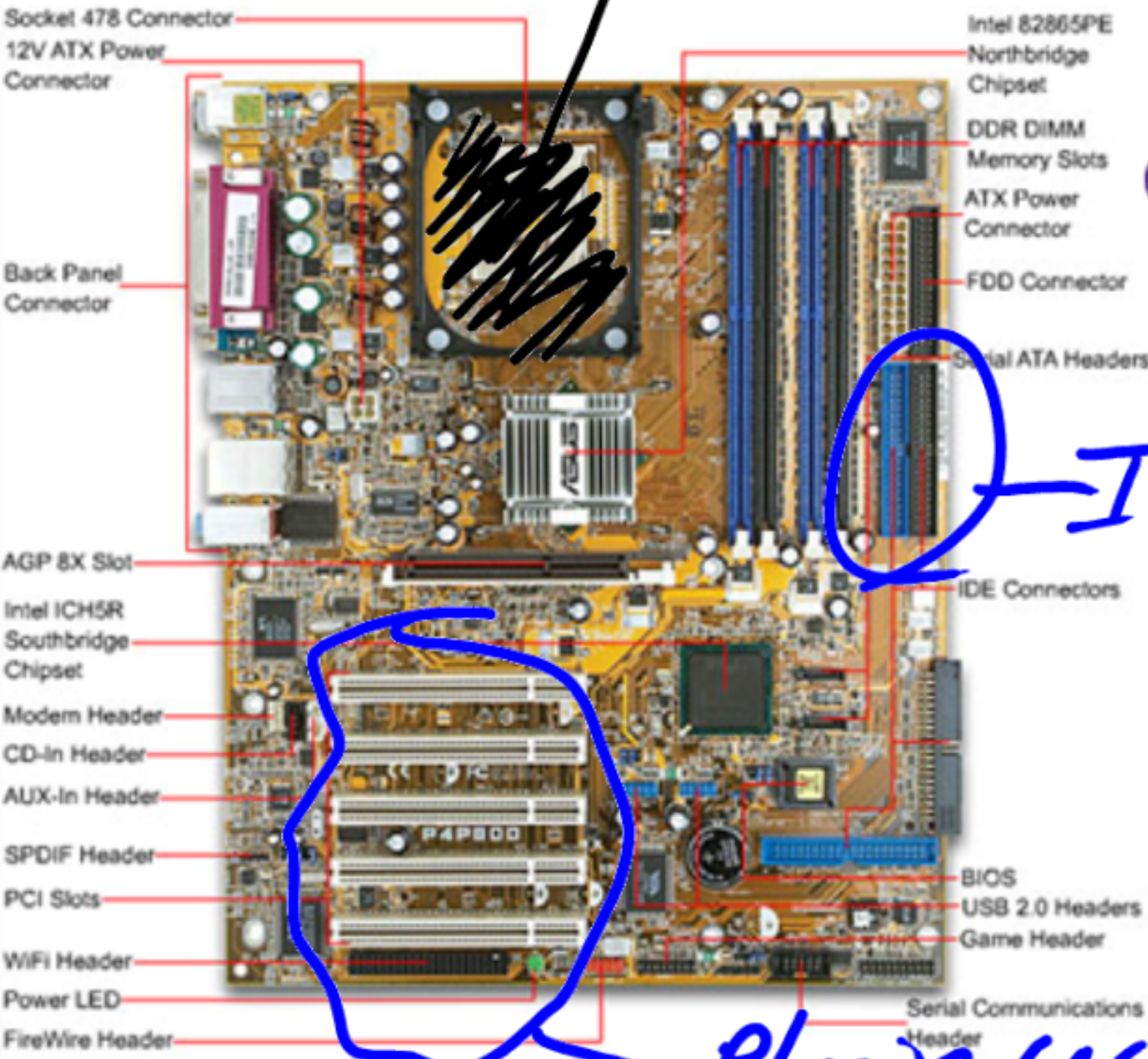
b. Software only design

c. Designed to run on a general purpose computer

d. A combination of hardware and software

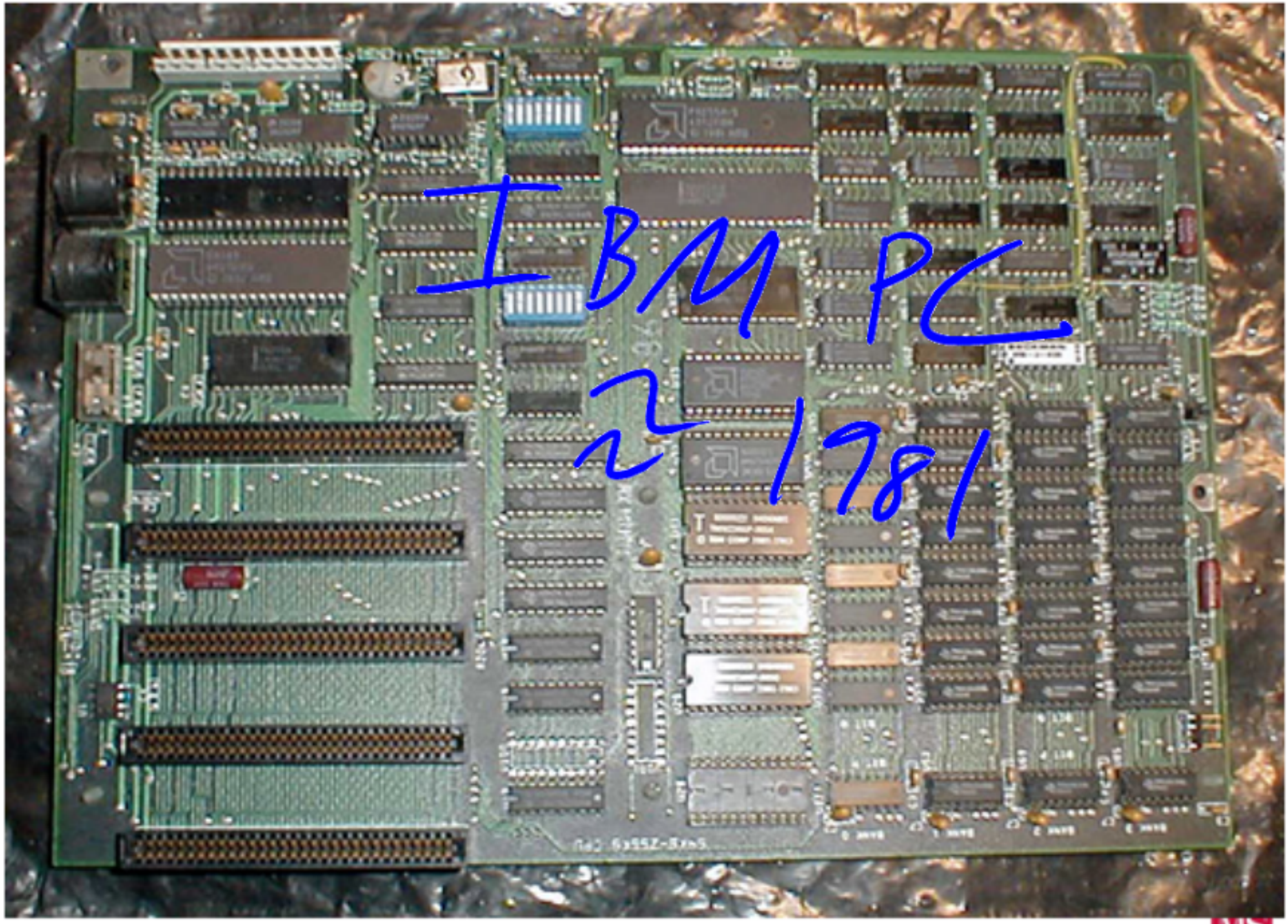
e. Always written in C++

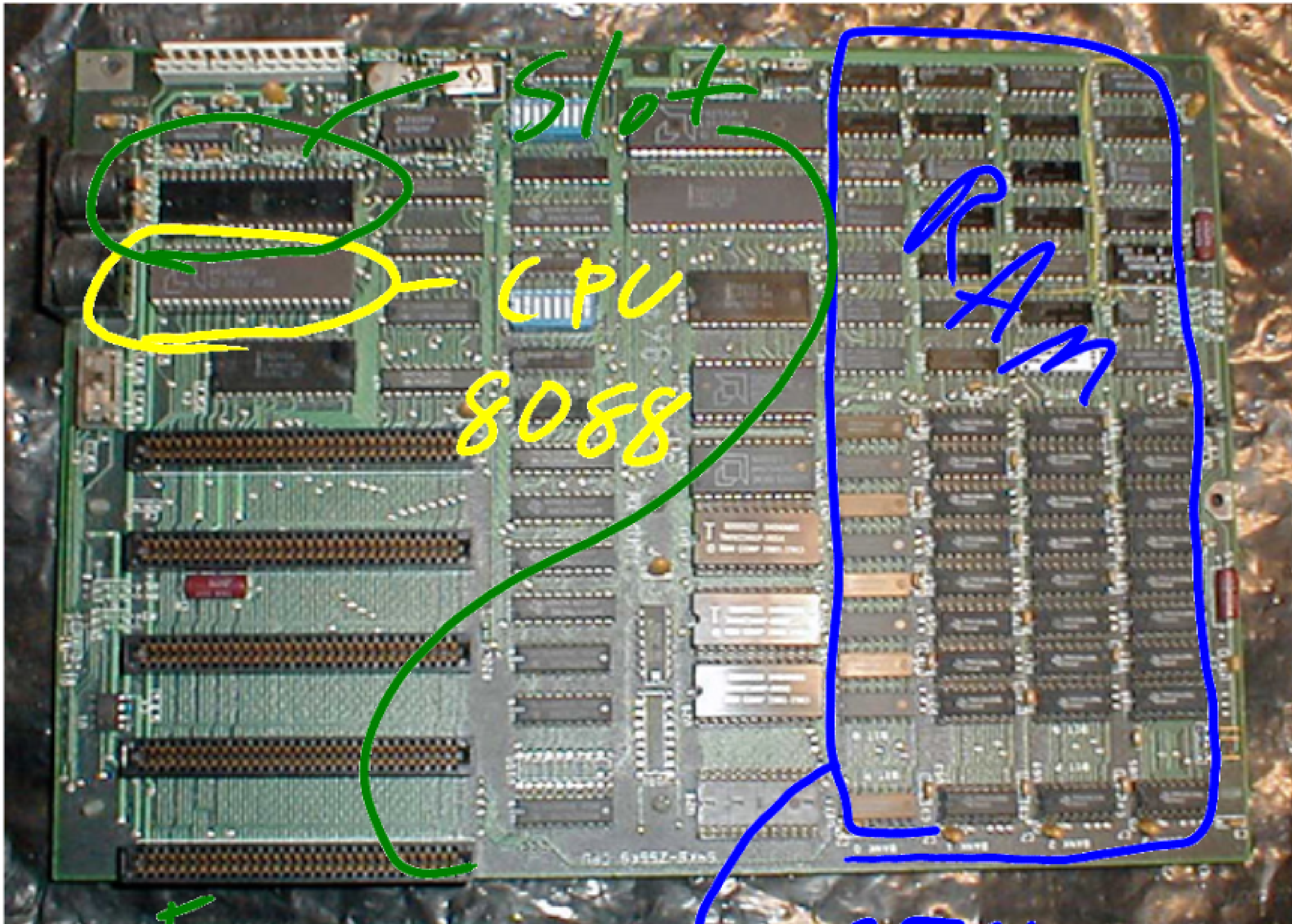
PARTS OF A GP COMPUTER (MICROCOMPUTER)



Contains separate

- Microprocessor(s)
- Memory
- Peripheral (I/O) device HW
  - serial port
  - parallel port
  - USB port
  - Bluetooth port
  - IR port
  - AGP port
  - WiFi port, …

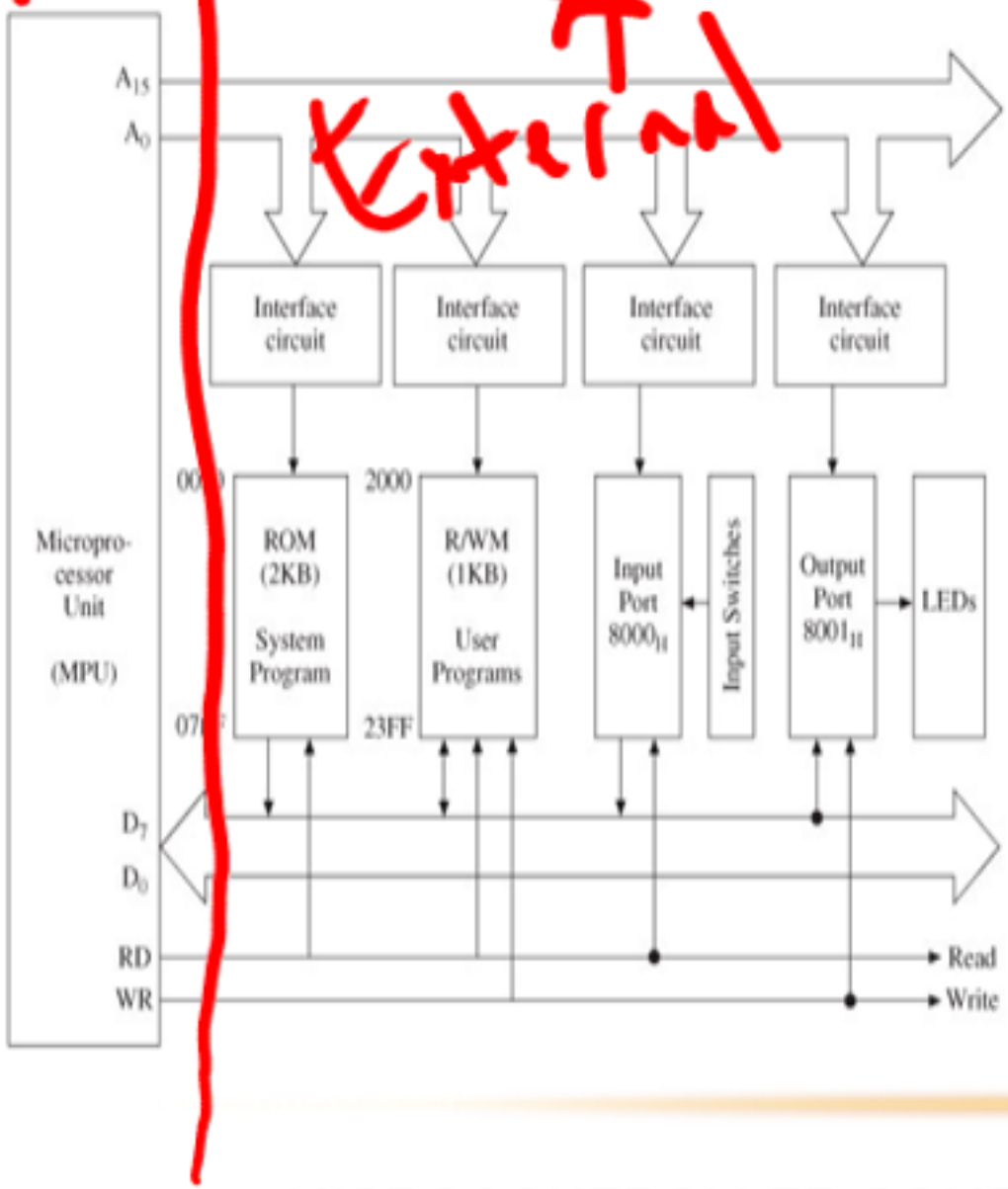

IBM PC
1981

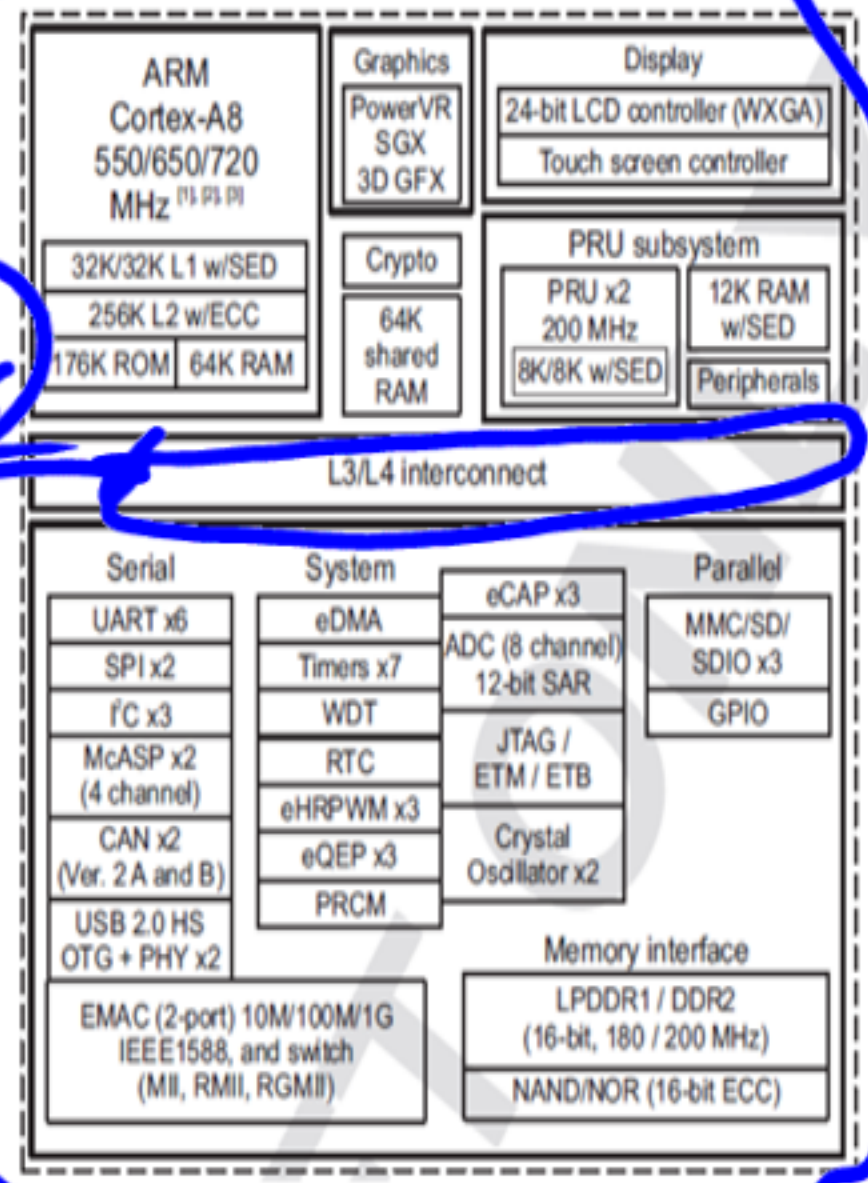

Slot
CPU
8088
RAM
256K
For a
Floating point Coprocessor

HOW DOES A MICROCOMPUTER DIFFER FROM A MICROCONTROLLER?

- Microcontroller
  - "1-chip" solution (monolithic)
    - Built-in components (depending on variant)
      - Microprocessor
      - Memory: RAM/SRAM, EEPROM/EPROM/PROM/ROM
      - Peripheral devices
        - serial/parallel ports
        - digital I/O ports
        - Analog/Digital converter
        - Timer/Counter

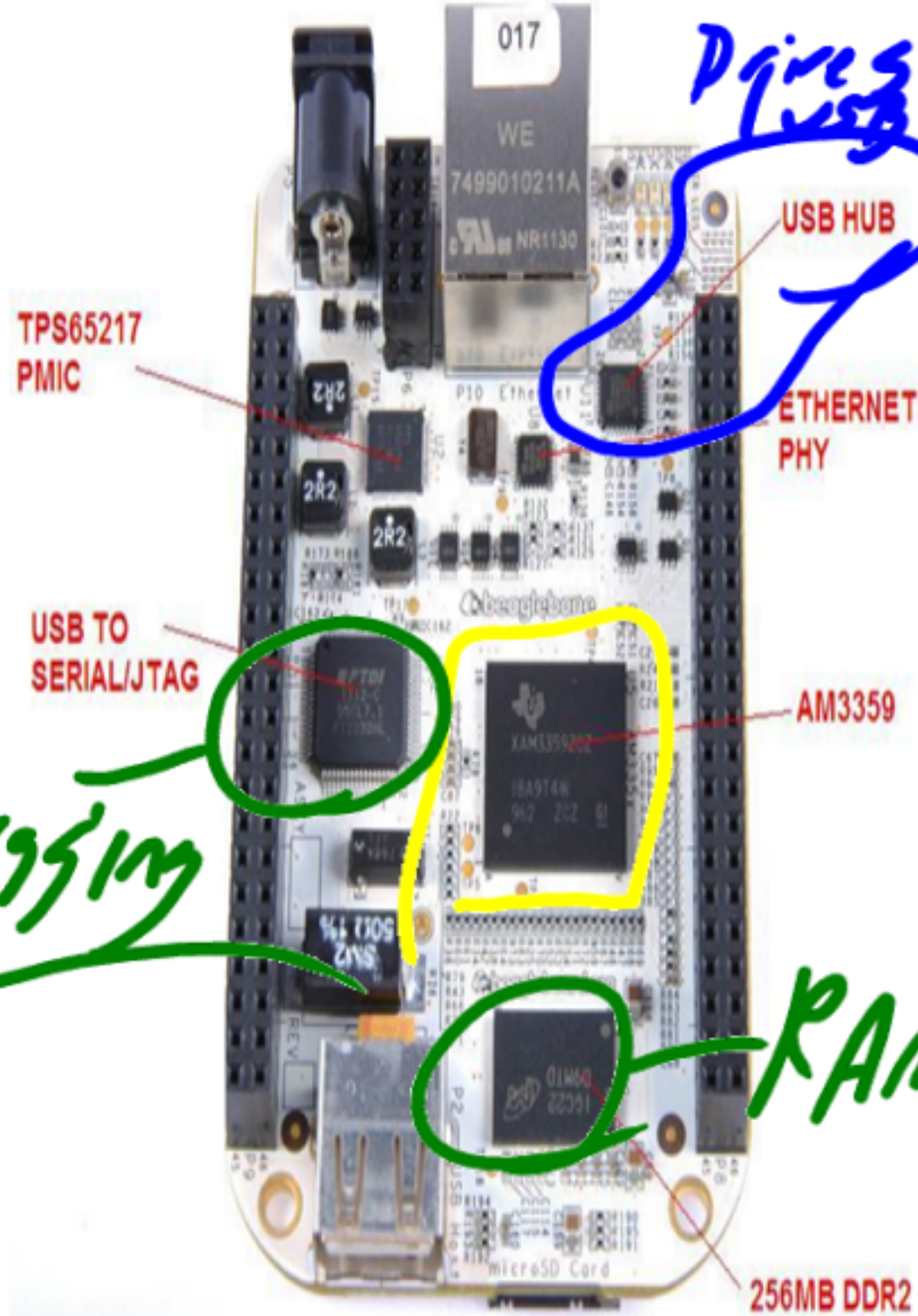
MICROPROCESSOR VERSUS MICROCONTROLLER





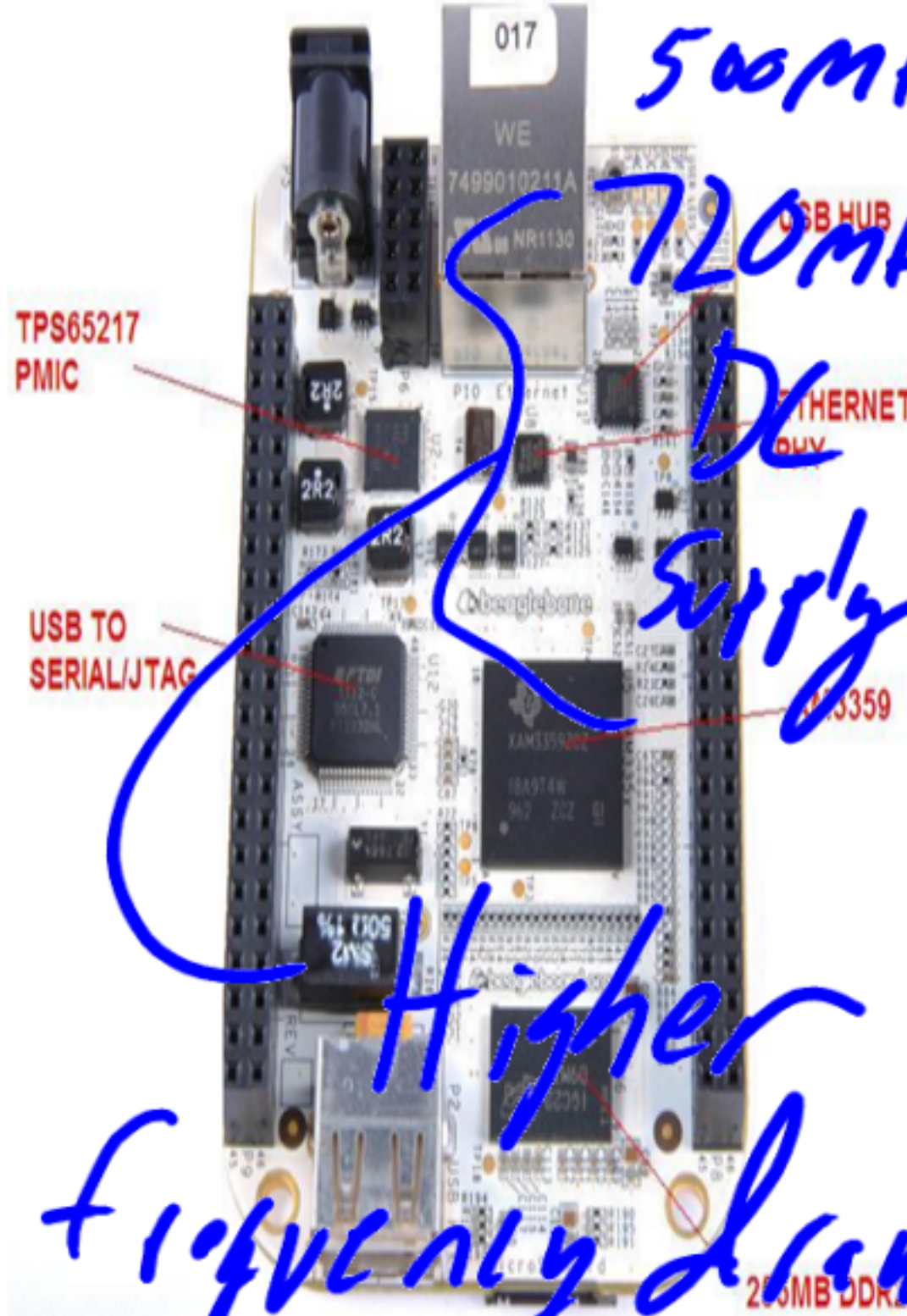
MICROCONTROLLER COMPONENTS

BEAGLEBONE



Feature		
Processor	AM3359 500MHZ-USB Powered 720MHZ-DC Powered	
Memory	256MB DDR2 400MHZ (128MB Optional)	
PMIC TPS65217B	Power Regulators	
	LiION Single cell battery charger (via expansion*)	
	20mA LED Backlight driver, 39V, PWM (via expansion*)	
	*(Additional components required)	
Debug Support	USB to Serial Adapter	miniUSB connector
	On Board JTAG via USB	4 USER LEDs
		Optional 20-pin CTI JTAG
Power	USB	5VDC External jack
PCB	3.4" x 2.1"	6 layers
Indicators	Power	
	4-User Controllable LEDs	
HS USB 2.0 Client Port	Access to the USB1 Client mode	
HS USB 2.0 Host Port	USB Type A Socket, 500mA LS/FS/HS	
Ethernet	10/100, RJ45	
SD/MMC Connector	microSD , 3.3V	
User Interface	1-Reset Button	
Overvoltage Protection	Shutdown @ 5.6V MAX	
Expansion Connectors	Power 5V, 3.3V , VDD_ADC(1.8V) 3.3V I/O on all signals McASP0, SPI1, I2C, GPIO(65), LCD, GPMC, MMC1, MMC2, 7 AIN(1.8V MAX), 4 Timers, 3 Serial Ports, CAN0, EHRPWM(0,2),XDMA Interrupt, Power button, Battery Charger, LED Backlight, Expansion Board ID (Up to 3 can be stacked)	
5V Power	USB or 5.0VDC to 5.2VDC See Table 3 for power consumption numbers.	
Weight	1.4 oz (39.68 grams)	

BEAGLEBONE



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V Power	USB or 5.0VDC to 5.2VDC See Table 3 for power consumption numbers.	
Weight	1.4 oz (39.68 grams)	

500mHz USB
720mHz
DC
Supply
Higher
frequency draws
more power

TI SITARA AM335 ARM CORTEX

1 Device Summary

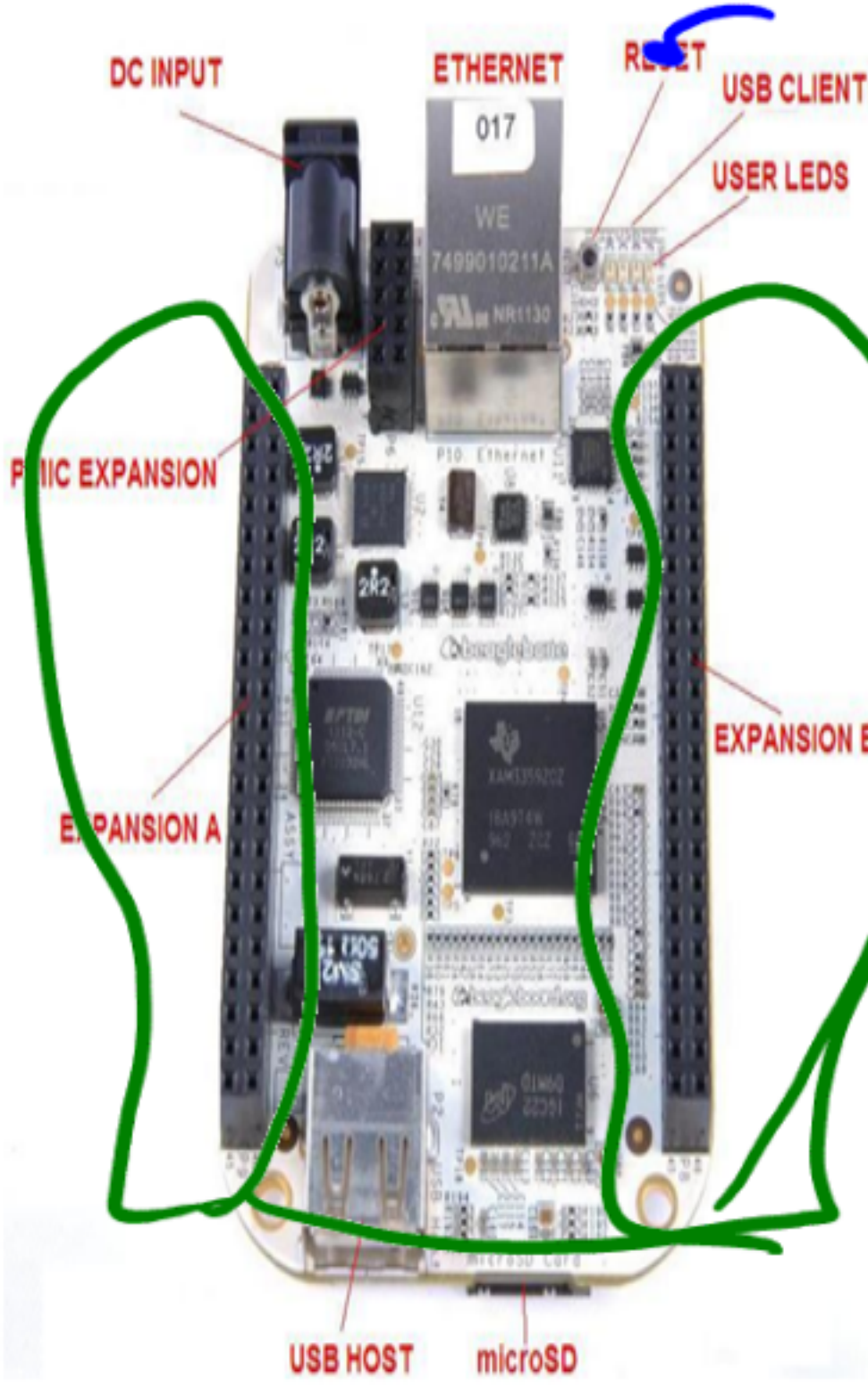
1.1 Features

- Highlights
  - Up to 1-GHz Sitara™ ARM® Cortex™-A8 32-Bit RISC Microprocessor
    - NEON™ SIMD Coprocessor
    - 32KB of L1 Instruction and 32KB Data Cache with Single-Error Detection (parity)
    - 256KB of L2 Cache with Error Correcting Code (ECC)
  - mDDR(LPDDR), DDR2, DDR3, DDR3L Support
  - General-Purpose Memory Support (NAND, NOR, SRAM) Supporting Up to 16-bit ECC
  - SGX530 3D Graphics Engine
  - LCD and Touchscreen Controller
  - Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
  - Real-Time Clock (RTC)
  - Up to Two USB 2.0 High-Speed OTG Ports with Integrated PHY
  - 10, 100, 1000 Ethernet Switch Supporting Up to Two Ports
  - Serial Interfaces Including:
    - Two Controller Area Network Ports (CAN)
    - Six UARTs, Two McASPs, Two McSPI, and Three I2C Ports
  - 12-Bit Successive Approximation Register (SAR) ADC
  - Up to Three 32-Bit Enhanced Capture Modules (eCAP)
  - Up to Three Enhanced High-Resolution PWM Modules (eHRPWM)
  - Crypto Hardware Accelerators (AES, SHA, PKA, RNG)

- MPU Subsystem
  - Up to 1-GHz ARM® Cortex™-A8 32-Bit RISC Microprocessor
  - NEON™ SIMD Coprocessor
  - 32KB of L1 Instruction Cache with Single-Error Detection (parity)
  - 32KB of L1 Data Cache with Single Error-Detection (parity)
  - 256KB of L2 Cache with Error Correcting Code (ECC)
  - 176KB of On-Chip Boot ROM
  - 64KB of Dedicated RAM
  - Emulation and Debug
    - JTAG
  - Interrupt Controller (up to 128 interrupt requests)
- On-Chip Memory (Shared L3 RAM)
  - 64 KB of General-Purpose On-Chip Memory Controller (OCMC) RAM
  - Accessible to all Masters
  - Supports Retention for Fast Wake-Up
- External Memory Interfaces (EMIF)
  - mDDR(LPDDR), DDR2, DDR3, DDR3L Controller:
    - mDDR: 200-MHz Clock (400-MHz Data Rate)
    - DDR2: 266-MHz Clock (532-MHz Data Rate)
    - DDR3: 400-MHz Clock (800-MHz Data Rate)
    - DDR3L: 400-MHz Clock (800-MHz Data Rate)
    - 16-Bit Data Bus
    - 1 GB of Total Addressable Space
    - Supports One x16 or Two x8 Memory Device Configurations
  - General-Purpose Memory Controller (GPMC)
    - Flexible 8-Bit and 16-Bit Asynchronous Memory Interface with Up to seven Chip Selects (NAND, NOR, Muxed-NOR, SRAM)
    - Uses BCH Code to Support 4-Bit, 8-Bit, or 16-Bit ECC
    - Uses Hamming Code to Support 1-Bit ECC
  - Error Locator Module (ELM)
    - Used in Conjunction with the GPMC to
    - 1-Bit, 4-Bit and 8-Bit MMC, SD, and SDIO Modes
    - MMCSD0 has dedicated Power Rail for 1.8-V or 3.3-V Operation
    - Up to 48-MHz Data Transfer Rate
    - Supports Card Detect and Write Protect
    - Complies with MMC4.3 and SD and SDIO 2.0 Specifications
  - Up to Three I2C Master and Slave Interfaces
    - Standard Mode (up to 100 kHz)
    - Fast Mode (up to 400 kHz)
  - Up to Four Banks of General-Purpose IO (GPIO)
    - 32 GPIOs per Bank (Multiplexed with Other Functional Pins)
    - GPIOs Can be Used as Interrupt Inputs (Up to Two Interrupt Inputs per Bank)
    - Up to Three External [illegible] Can Also be Used as Interrupt Inputs
  - Eight 32-Bit General-Purpose Timers
    - DMTIMER1 is a 1-ms Timer Used for Operating System (OS) Ticks
    - DMTIMER4 - DMTIMER7 are Pinned Out
  - One Watchdog Timer
  - SGX530 3D Graphics Engine
    - Tile-Based Architecture Delivering Up to 20 Million Polygons per second
    - Universal Scalable Shader Engine is a Multi-Threaded Engine Incorporating Pixel and Vertex Shader Functionality
    - Advanced Shader Feature Set in Excess of Microsoft VS3.0, PS3.0 and OGL2.0
    - Industry Standard API Support of Direct3D Mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0, and OpenMax
    - Fine-Grained Task Switching, Load Balancing and Power Management
    - Advanced Geometry DMA Driven Operation for Minimum CPU Interaction
    - Programmable High-Quality Image Anti-Aliasing
    - Fully Virtualized Memory Addressing for OS Operation in a Unified Memory Architecture
  - LCD Controller
    - Up to 24-Bits Data Output; 8-Bits per Pixel (RGB)
    - Resolution Up to 2048x2048 (With Maximum 126-MHz Pixel Clock)
    - Integrated LCD Interface Display Driver (LIDD) Controller
    - Integrated Raster Controller
    - Integrated DMA Engine to Pull Data from the External Frame Buffer without Burdening the Processor via Interrupts or a Firmware Timer
    - 512-Word Deep Internal FIFO
    - Supported Display Types:
      - Character Displays - Uses LCD Interface Display Driver (LIDD) Controller to Program these Displays
      - Passive Matrix LCD Displays - Uses LCD Raster Display Controller to Provide Timing and Data for Constant Graphics Refresh to a Passive Display
      - Active Matrix LCD Displays - Uses External Frame Buffer Space and the Internal DMA Engine to Drive Streaming Data to the Panel
  - 12-Bit Successive Approximation Register (SAR) ADC
    - 200K Samples per Second
    - Input Can be Selected from any of the Eight Analog Inputs Multiplexed Through an 8:1 analog Switch
    - Can be Configured to Operate as a 4-wire, 5-wire, or 8-wire Resistive Touch Screen Controller (TSC) Interface
  - Up to Three 32-Bit Enhanced Capture Modules (eCAP)
    - Configurable as Three Capture Inputs or Three Auxiliary PWM Outputs
  - Up to Three Enhanced High-Resolution PWM Modules (eHRPWM)
    - Dedicated 16-Bit Time-Base Counter with Time and Frequency Controls
    - Configurable as Six Single-Ended, Six Dual-Edge Symmetric, or Three Dual-Edge Asymmetric Outputs
  - Up to Three 32-Bit Enhanced Quadrature Encoder Pulse (eQEP) Modules
- Device Identification
  - Contains Electrical fuse Farm (FuseFarm) of Which Some Bits are Factory Programmable
    - Production ID
    - Device Part Number (Unique JTAG ID)
    - Device Revision (readable by Host ARM)
- Debug Interface Support
  - JTAG and cJTAG for ARM (Cortex-A8 and PRCM), PRU-ICSS Debug
  - Supports Device Boundary Scan
  - Supports IEEE 1500
- DMA
  - On-Chip Enhanced DMA Controller (EDMA) has Three Third-Party Transfer Controllers (TPTC) and One Third-Party Channel Controller (TPCC), Which Supports Up to 64 Programmable Logical Channels and Eight QDMA Channels. EDMA is Used for:
    - Transfers to and from On-Chip Memories

SE3910 REAL TIME SYSTEMS

BEAGLEBONE EXPANSION



GPIO Expansion

General purpose I/O

2 USB devices { Hub

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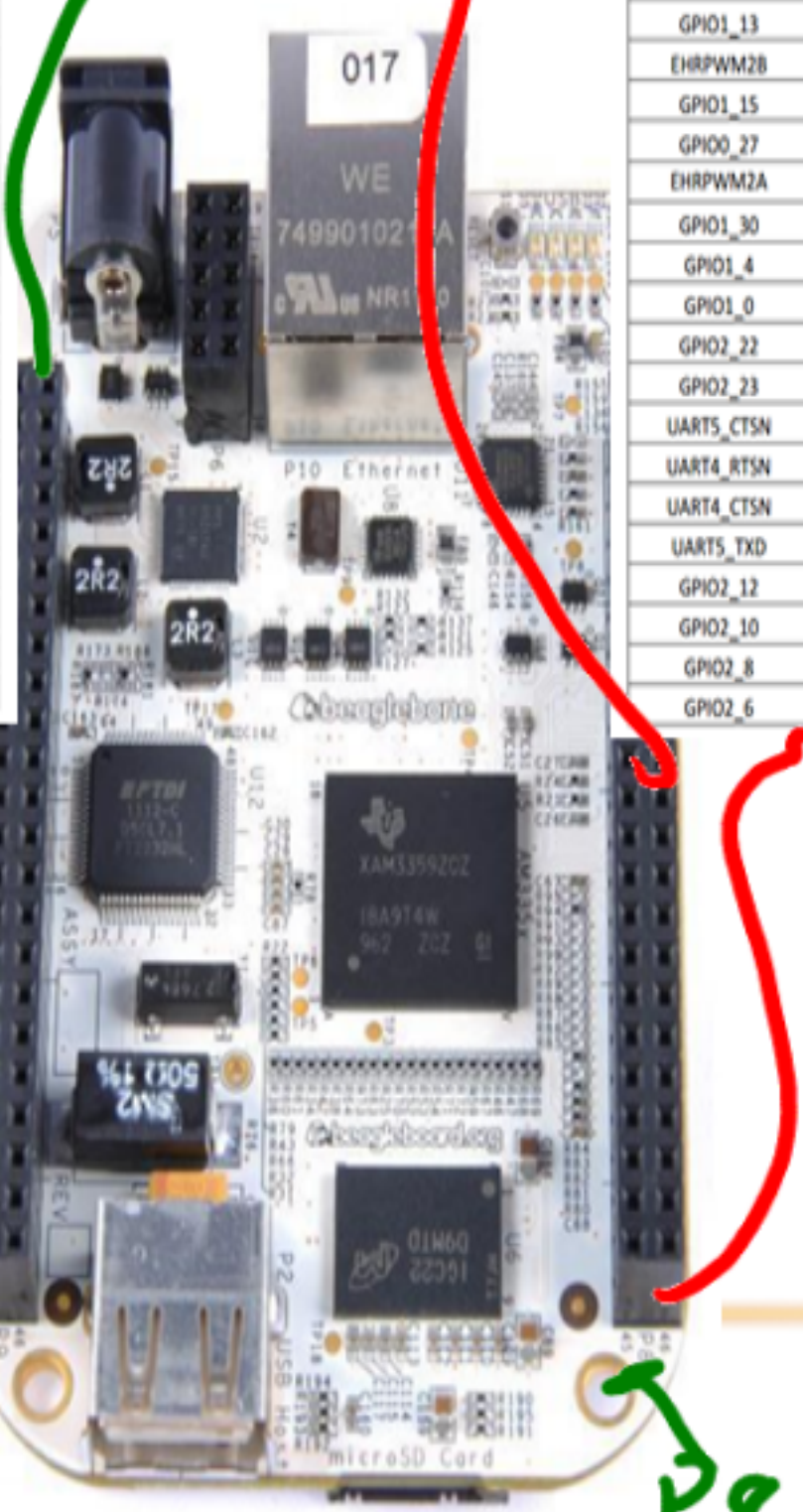
EXPANSION PORTS

Table 11. Expansion Header P9 Pinout

SIGNAL NAME	PIN	CONN		PIN	SIGNAL NAME
	GND	1	2	GND	
	VDD_3V3EXP	3	4	VDD_3V3EXP	
	VDD_5V	5	6	VDD_5V	
	SYS_5V	7	8	SYS_5V	
PWR_BUT*		9	10	A10	SYS_RESETn
UART4_RXD	T17	11	12	U18	GPIO1_28
UART4_TXD	U17	13	14	U14	EHRPWM1A
GPIO1_16	R13	15	16	T14	EHRPWM1B
I2C1_SCL	A16	17	18	B16	I2C1_SDA
I2C2_SCL	D17	19	20	D18	I2C2_SDA
UART2_TXD	B17	21	22	A17	UART2_RXD
GPIO1_17	V14	23	24	D15	UART1_TXD
GPIO3_21	A14	25	26	D16	UART1_RXD
GPIO3_19	C13	27	28	C12	SPI1_CS0
SPI1_D0	B13	29	30	D12	SPI1_D1
SPI1_SCLK	A13	31	32	VDD_ADC(1.8V)	
AIN4	C8	33	34	GNDA_ADC	
AIN6	A5	35	36	A5	AIN5
AIN2	B7	37	38	A7	AIN3
AIN0	B6	39	40	C7	AIN1
CLKOUT2	D14	41	42	C18	GPIO0_7
	GND	43	44	GND	
	GND	45	46	GND	

Table 8. Expansion Header P8 Pinout

SIGNAL NAME	PROC	CONN		PROC	SIGNAL NAME
	GND	1	2	GND	
GPIO1_6	R9	3	4	T9	GPIO1_7
GPIO1_2	R8	5	6	T8	GPIO1_3
TIMER4	R7	7	8	T7	TIMER7
TIMER5	T6	9	10	U6	TIMER6
GPIO1_13	R12	11	12	T12	GPIO1_12
EHRPWM2B	T10	13	14	T11	GPIO0_26
GPIO1_15	U13	15	16	V13	GPIO1_14
GPIO0_27	U12	17	18	V12	GPIO2_1
EHRPWM2A	U10	19	20	V9	GPIO1_31
GPIO1_30	U9	21	22	V8	GPIO1_5
GPIO1_4	U8	23	24	V7	GPIO1_1
GPIO1_0	U7	25	26	V6	GPIO1_29
GPIO2_22	U5	27	28	V5	GPIO2_24
GPIO2_23	R5	29	30	R6	GPIO2_25
UART5_CTSN	V4	31	32	T5	UART5_RTSN
UART4_RTSN	V3	33	34	U4	UART3_RTSN
UART4_CTSN	V2	35	36	U3	UART3_CTSN
UART5_TXD	U1	37	38	U2	UART5_RXD
GPIO2_12	T3	39	40	T4	GPIO2_13
GPIO2_10	T1	41	42	T2	GPIO2_11
GPIO2_8	R3	43	44	R4	GPIO2_9
GPIO2_6	R1	45	46	R2	GPIO2_7



P1

P8

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EXPANSION PORTS

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SIGNAL NAME	PIN	CONN		PIN	SIGNAL NAME
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	VDD_5V	5	6	VDD_5V	
	SYS_5V	7	8	SYS_5V	
PWR_BUT*		9	10	A10	SYS_RESETn
UART4_RXD	T17	11	12	U18	GPIO1_28
UART4_TXD	U17	13	14	U14	EHRPWM1A
GPIO1_16	R13	15	16	T14	EHRPWM1B
I2C1_SCL	A16	17	18	B16	I2C1_SDA
I2C2_SCL	D17	19	20	D18	I2C2_SDA
UART2_TXD	B17	21	22	A17	UART2_RXD
GPIO1_17	V14	23	24	D15	UART1_TXD
GPIO3_21	A14	25	26	D16	UART1_RXD
GPIO3_19	C13	27	28	C12	SPI1_CS0
SPI1_D0	B13	29	30	D12	SPI1_D1
SPI1_SCLK	A13	31	32	VDD_ADC(1.8V)	
AIN4	C8	33	34	GNDA_ADC	
AIN6	A5	35	36	A5	AIN5
AIN2	B7	37	38	A7	AIN3
AIN0	B6	39	40	C7	AIN1
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GND

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TIMER4	R7	7	8	T7	TIMER7
TIMER5	T6	9	10	U6	TIMER6
GPIO1_13	R12	11	12	T12	GPIO1_12
EHRPWM2B	T10	13	14	T11	GPIO0_26
GPIO1_15	U13	15	16	V13	GPIO1_14
GPIO0_27	U12	17	18	V12	GPIO2_1
EHRPWM2A	U10	19	20	V9	GPIO1_31
GPIO1_30	U9	21	22	V8	GPIO1_5
GPIO1_4	U8	23	24	V7	GPIO1_1
GPIO1_0	U7	25	26	V6	GPIO1_29
GPIO2_22	U5	27	28	V5	GPIO2_24
GPIO2_23	R5	29	30	R6	GPIO2_25
UART5_CTSN	V4	31	32	T5	UART5_RTSN
UART4_RTSN	V3	33	34	U4	UART3_RTSN
UART4_CTSN	V2	35	36	U3	UART3_CTSN
UART5_TXD	U1	37	38	U2	UART5_RXD
GPIO2_12	T3	39	40	T4	GPIO2_13
GPIO2_10	T1	41	42	T2	GPIO2_11
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12, 14, 16

44 26 46

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EXPANSION PORTS

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I2C2_SCL	D17	19	20	D18	I2C2_SDA
UART2_TXD	B17	21	22	A17	UART2_RXD
GPIO1_17	V14	23	24	D15	UART1_TXD
GPIO3_21	A14	25	26	D16	UART1_RXD
GPIO3_19	C13	27	28	C12	SPI1_CS0
SPI1_D0	B13	29	30	D12	SPI1_D1
SPI1_SCLK	A13	31	32	VDD_ADC(1.8V)	
AIN4	C8	33	34	GNDA_ADC	
AIN6	A5	35	36	A5	AIN5
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	GND	43	44	GND	
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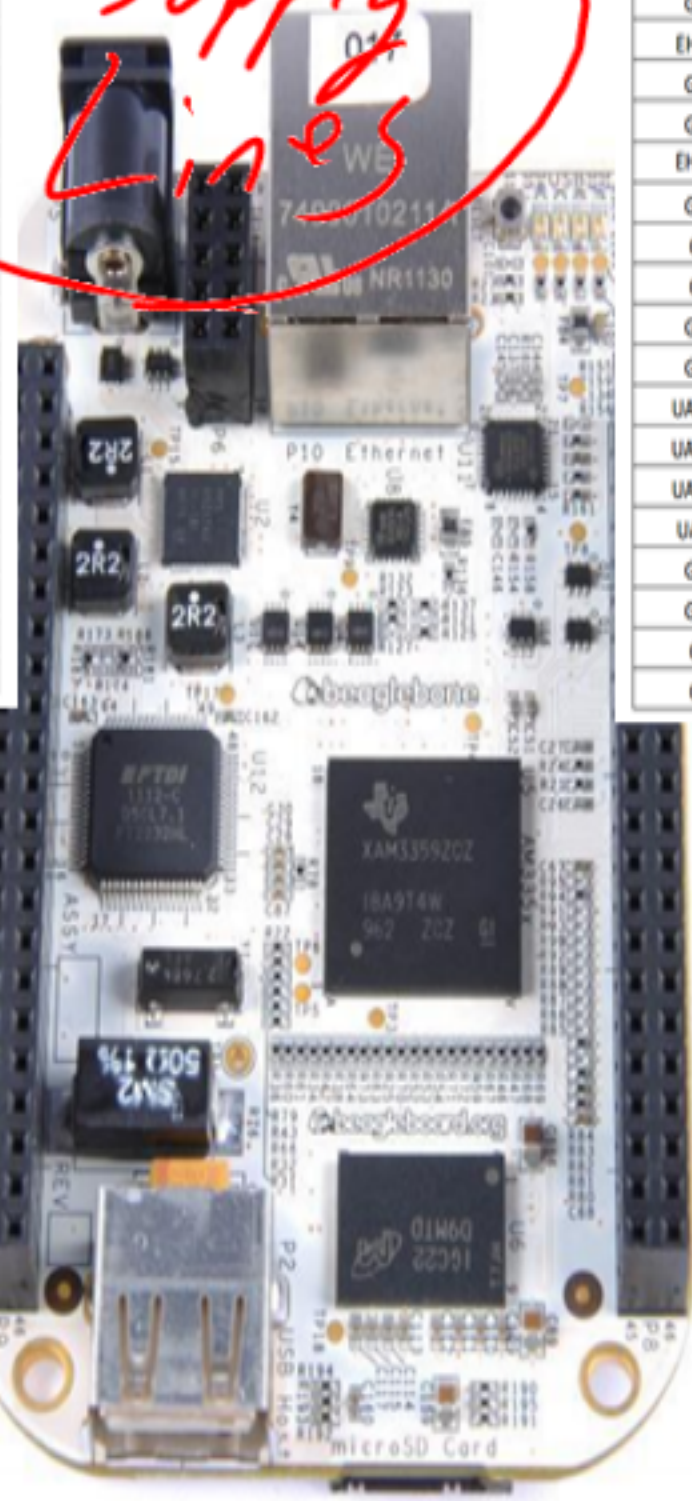
Power Supply Lines



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TIMER4	R7	7	8	T7	TIMER7
TIMER5	T6	9	10	U6	TIMER6
GPIO1_13	R12	11	12	T12	GPIO1_12
EHRPWM2B	T10	13	14	T11	GPIO0_26
GPIO1_15	U13	15	16	V13	GPIO1_14
GPIO0_27	U12	17	18	V12	GPIO2_1
EHRPWM2A	U10	19	20	V9	GPIO1_31
GPIO1_30	U9	21	22	V8	GPIO1_5
GPIO1_4	U8	23	24	V7	GPIO1_1
GPIO1_0	U7	25	26	V6	GPIO1_29
GPIO2_22	U5	27	28	V5	GPIO2_24
GPIO2_23	R5	29	30	R6	GPIO2_25
UART5_CTSN	V4	31	32	T5	UART5_RTSN
UART4_RTSN	V3	33	34	U4	UART3_RTSN
UART4_CTSN	V2	35	36	U3	UART3_CTSN
UART5_TXD	U1	37	38	U2	UART5_RXD
GPIO2_12	T3	39	40	T4	GPIO2_13
GPIO2_10	T1	41	42	T2	GPIO2_11
GPIO2_8	R3	43	44	R4	GPIO2_9
GPIO2_6	R1	45	46	R2	GPIO2_7

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CALCULATING THE GPIO PIN NUMBER

expansion header

Table 12. Expansion Header P8 Pinout

PIN	PROC	NAME	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MODE7
1,2						GND				
3	R9	GPIO1_6	gpmc_ad6	mmc1_dat6						gpio1[6]
4	T9	GPIO1_7	gpmc_ad7	mmc1_dat7						gpio1[7]
5	R8	GPIO1_2	gpmc_ad2	mmc1_dat2						gpio1[2]
6	T8	GPIO1_3	gpmc_ad3	mmc1_dat3						gpio1[3]
7	R7	TIMER4	gpmc_advn_ale		timer4					gpio2[2]
8	T7	TIMER7	gpmc_oen_ren		timer7					gpio2[3]
9	T6	TIMER5	gpmc_be0n_cle		timer5					gpio2[5]
10	U6	TIMER6	gpmc_wen		timer6					gpio2[4]
11	R12	GPIO1_13	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in		pr1_pru0_pru_r30_15	gpio1[13]
12	T12	GPIO1_12	gpmc_ad12	Lcd_data19	mmc1_dat4	Mmc2_dat0	Eqep2a_in		pr1_pru0_pru_r30_14	gpio1[12]
13	T10	EHRPWM2B	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpwm2B			gpio0[23]
14	T11	GPIO0_26	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpwm2_tripzone_in			gpio0[26]
15	U13	GPIO1_15	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe		pr1_pru0_pru_r31_15	gpio1[15]
16	V13	GPIO1_14	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index		pr1_pru0_pru_r31_14	gpio1[14]
17	U12	GPIO0_27	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpwm0_synco			gpio0[27]
18	V12	GPIO2_1	gpmc_clk_mux0	lcd_memory_clk	gpmc_wait1	mmc2_clk			mcasp0_fsr	gpio2[1]
19	U10	EHRPWM2A	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpwm2A			gpio0[22]
20	V9	GPIO1_31	gpmc_csn2	gpmc_be1n	mmc1_cmd			pr1_pru1_pru_r30_13	pr1_pru1_pru_r31_13	gpio1[31]
21	U9	GPIO1_30	gpmc_csn1	gpmc_clk	mmc1_clk			pr1_pru1_pru_r30_12	pr1_pru1_pru_r31_12	gpio1[30]
22	V8	GPIO1_5	gpmc_ad5	mmc1_dat5						gpio1[5]
23	U8	GPIO1_4	gpmc_ad4	mmc1_dat4						gpio1[4]
24	V7	GPIO1_1	gpmc_ad1	mmc1_dat1						gpio1[1]
25	U7	GPIO1_0	gpmc_ad0	mmc1_dat0						gpio1[0]
26	V6	GPIO1_29	gpmc_csn0							gpio1[29]
27	U5	GPIO2_22	lcd_vsync	gpmc_a8				pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio2[22]
28	V5	GPIO2_24	lcd_pclk	gpmc_a10				pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	gpio2[24]
29	R5	GPIO2_23	lcd_hsync	gpmc_a9				pr1_pru1_pru_r30_9	pr1_pru1_pru_r31_9	gpio2[23]
30	R6	GPIO2_25	lcd_ac_bias_en	gpmc_a11						gpio2[25]
31	V4	UART5_CTSN	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd		uart5_ctsn	gpio0[10]
32	T5	UART5_RTSN	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3		uart5_rtsn	gpio0[11]
33	V3	UART4_RTSN	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3		uart4_rtsn	gpio0[9]
34	U4	UART3_RTSN	lcd_data11	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2		uart3_rtsn	gpio2[17]
35	V2	UART4_CTSN	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2		uart4_ctsn	gpio0[8]
36	U3	UART3_CTSN	lcd_data10	gpmc_a14	ehrpwm1A	mcasp0_axr0			uart3_ctsn	gpio2[16]
37	U1	UART5_TXD	lcd_data8	gpmc_a12	ehrpwm1_tripzone_in	mcasp0_aclkx	uart5_txd		uart2_ctsn	gpio2[14]
38	U2	UART5_RXD	lcd_data9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd		uart2_rtsn	gpio2[15]
39	T3	GPIO2_12	lcd_data6	gpmc_a6		eQEP2_index		pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2[12]
40	T4	GPIO2_13	lcd_data7	gpmc_a7		eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2[13]
41	T1	GPIO2_10	lcd_data4	gpmc_a4		eQEP2A_in		pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2[10]
42	T2	GPIO2_11	lcd_data5	gpmc_a5		eQEP2B_in		pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2[11]
43	R3	GPIO2_8	lcd_data2	gpmc_a2		ehrpwm2_tripzone_in		pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio2[8]
44	R4	GPIO2_9	lcd_data3	gpmc_a3		ehrpwm0_synco		pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio2[9]
45	R1	GPIO2_6	lcd_data0	gpmc_a0		ehrpwm2A		pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio2[6]
46	R2	GPIO2_7	lcd_data1	gpmc_a1		ehrpwm2B		pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio2[7]

CALCULATING THE PIN NUMBER

32 pins/ Bank

- Up to Four Banks of General-Purpose IO (GPIO)
  - 32 GPIOs per Bank (Multiplexed with Other Functional Pins)
  - GPIOs Can be Used as Interrupt Inputs (Up to Two Interrupt Inputs per Bank)

$$Export\ Pin\ Number = GPIOControllerNumber * 32 + GPIOPin$$

GPIO1_12

1*32 + 12 = 44

- Up to Four Banks of General-Purpose IO (GPIO)
  - 32 GPIOs per Bank (Multiplexed with Other Functional Pins)
  - GPIOs Can be Used as Interrupt Inputs (Up to Two Interrupt Inputs per Bank)

CALCULATING THE PIN NUMBER

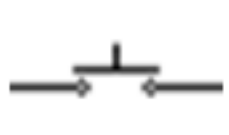
$$Export\ Pin\ Number = GPIOControllerNumber * 32 + GPIOPin$$

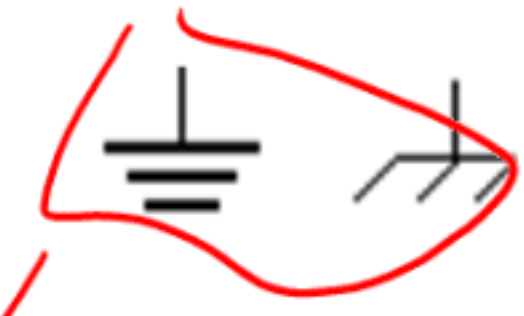
Pin 14 => GPIO0_26

0 * 32 + 26 => 26

INTRODUCTION TO SCHEMATICS

- Resistor 

- Switch 

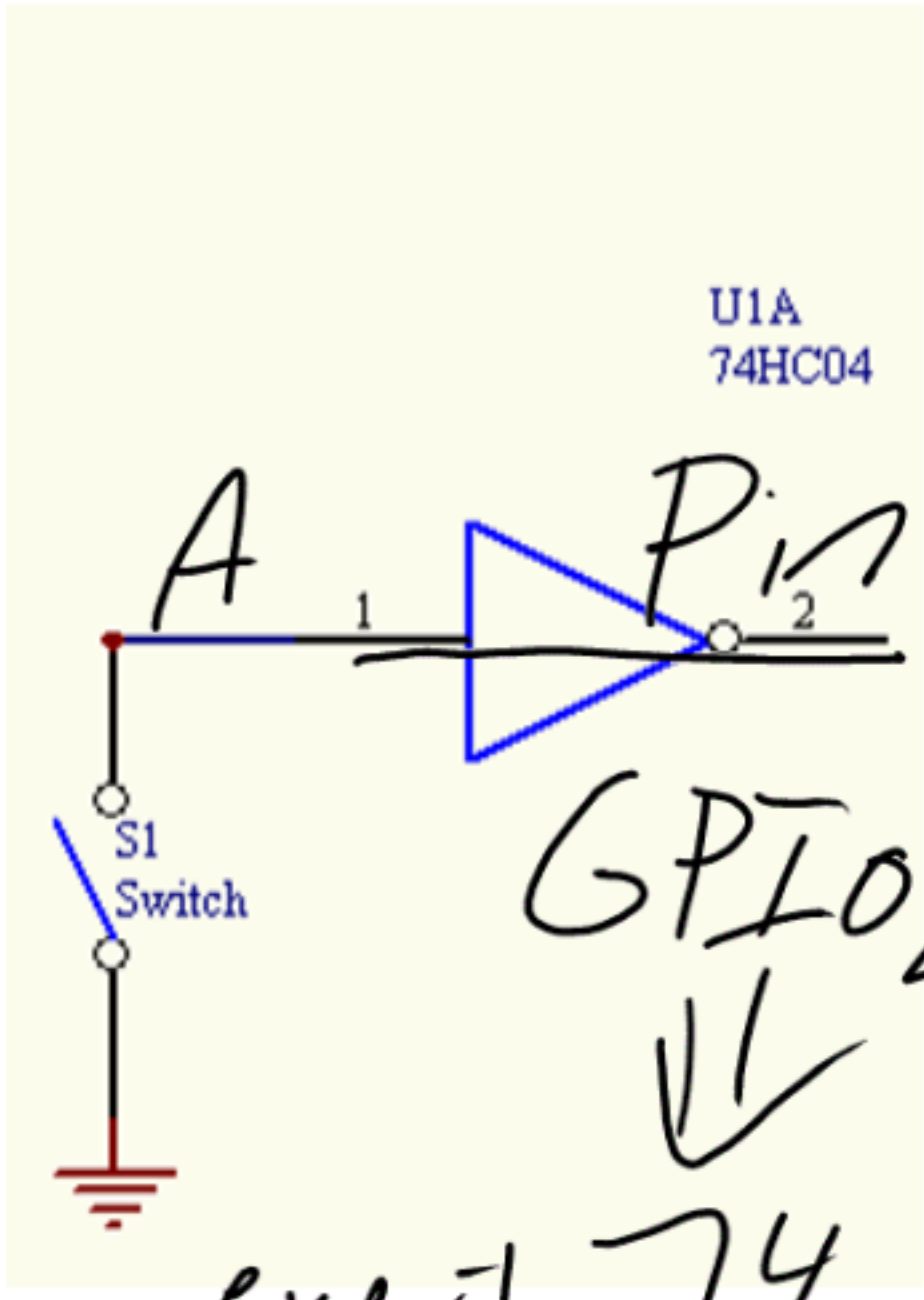
- Ground 

=> Resists Flow of Current

Opens/closes a circuit

Where things go

A SIMPLE INPUT CIRCUIT

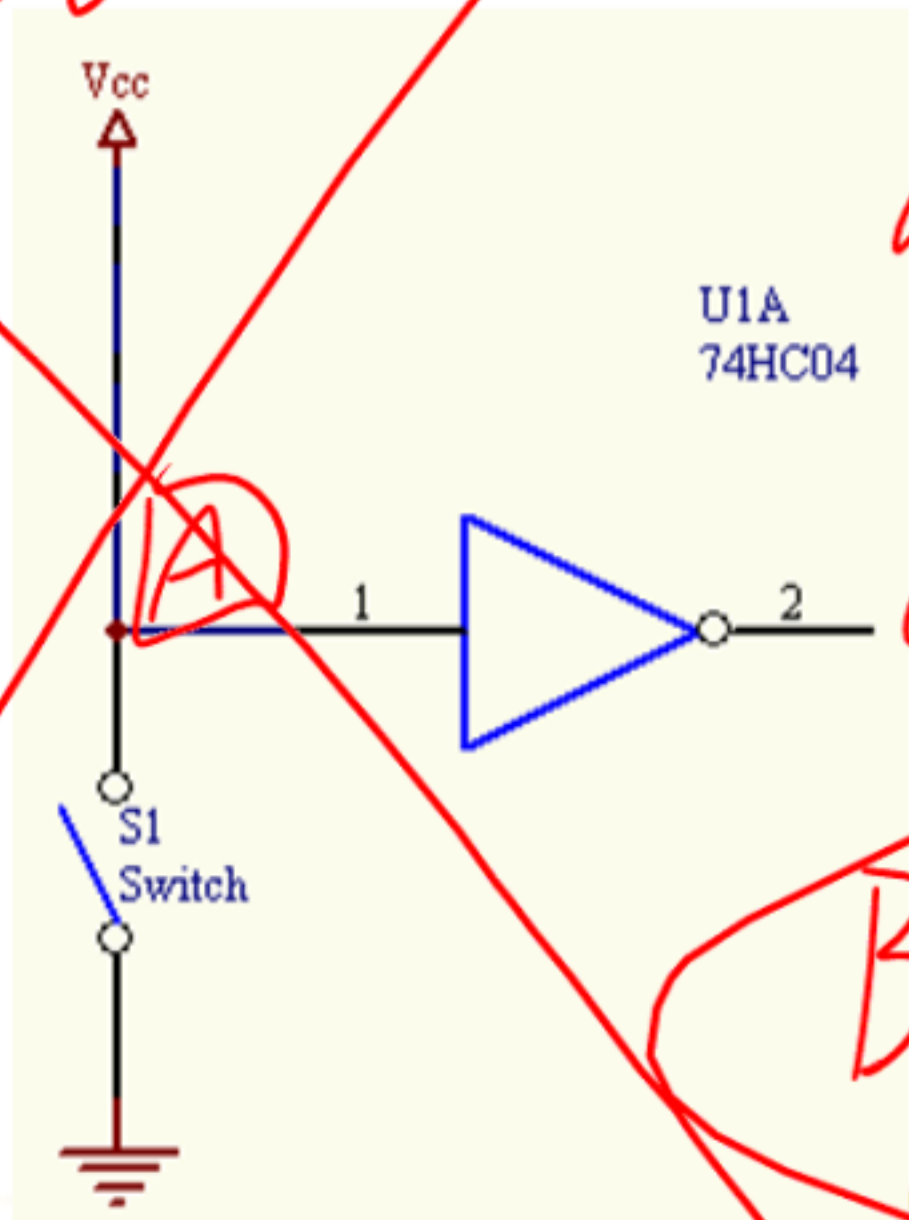


Switch open: A ?

Switch closed: A — Ground

Floating input

A SOLUTION?



5V

A

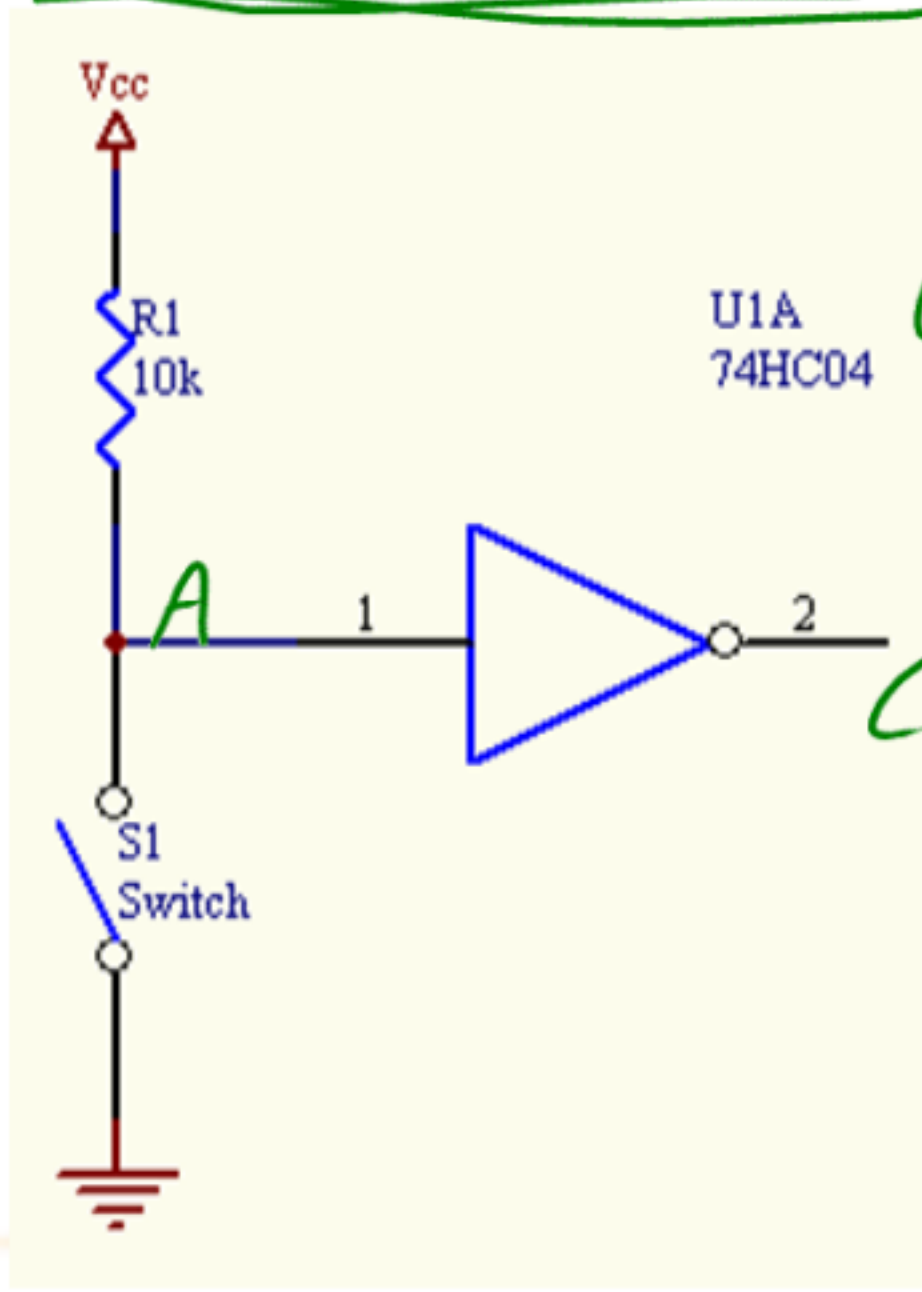
Open 2 3.3V Logic High

closed ⇒

But solution

A GOOD SOLUTION

Pull up resistor

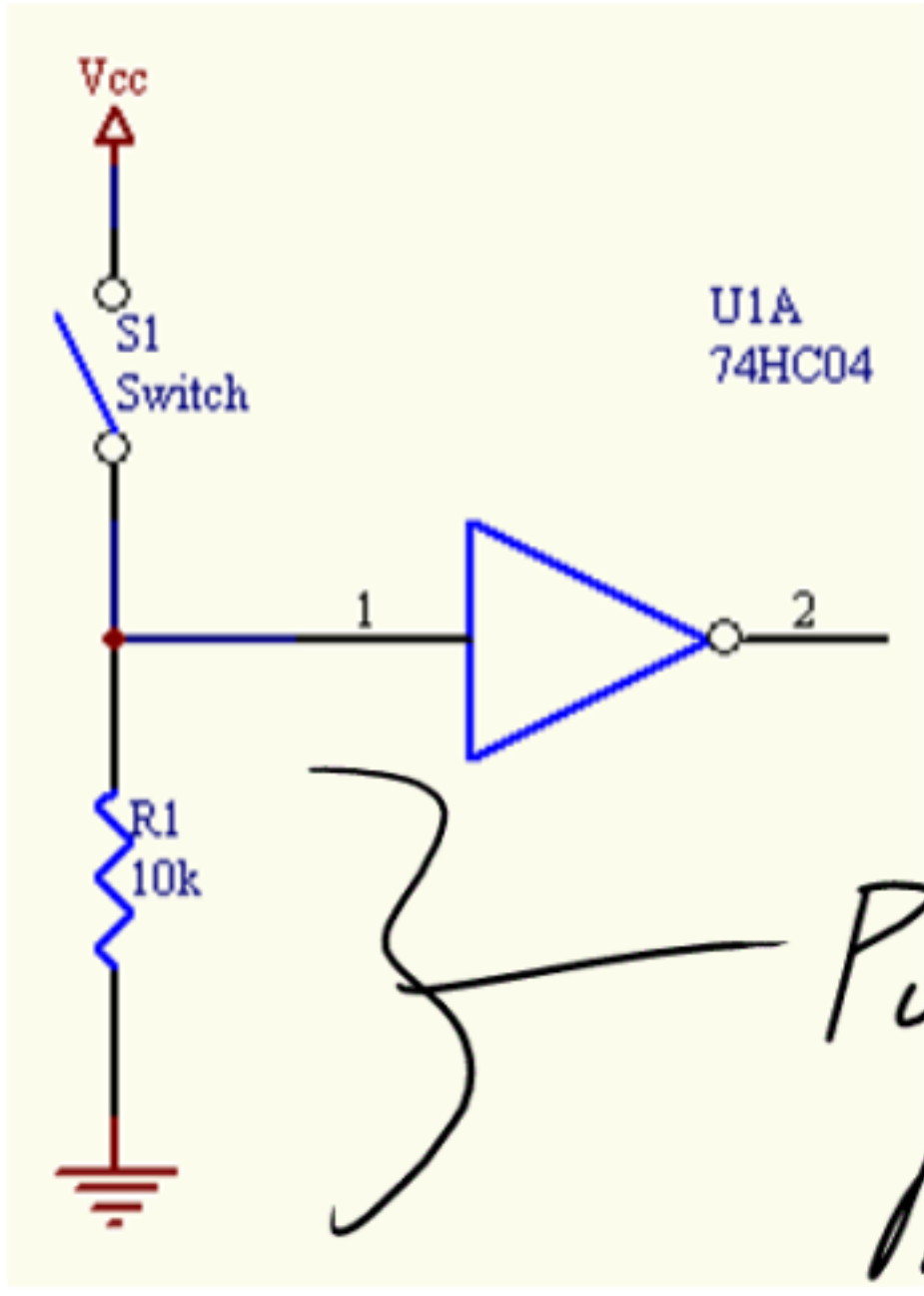


A

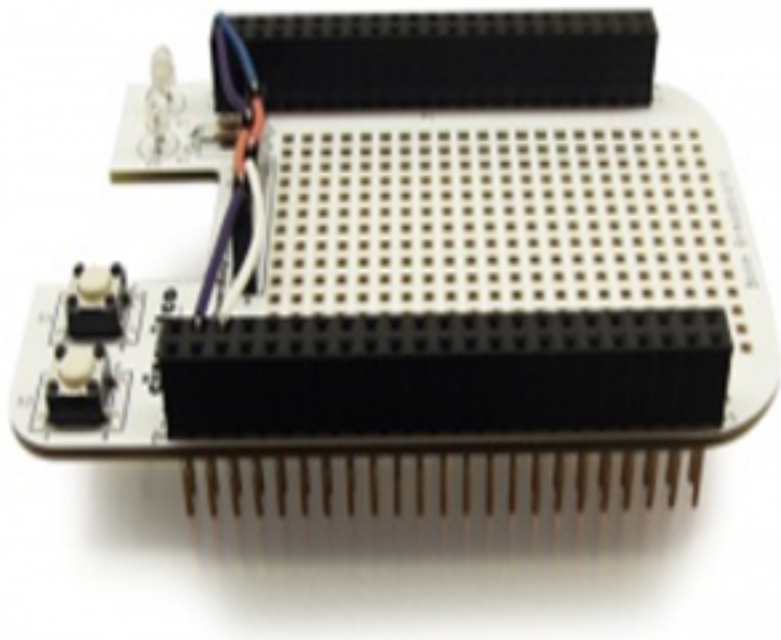
open High

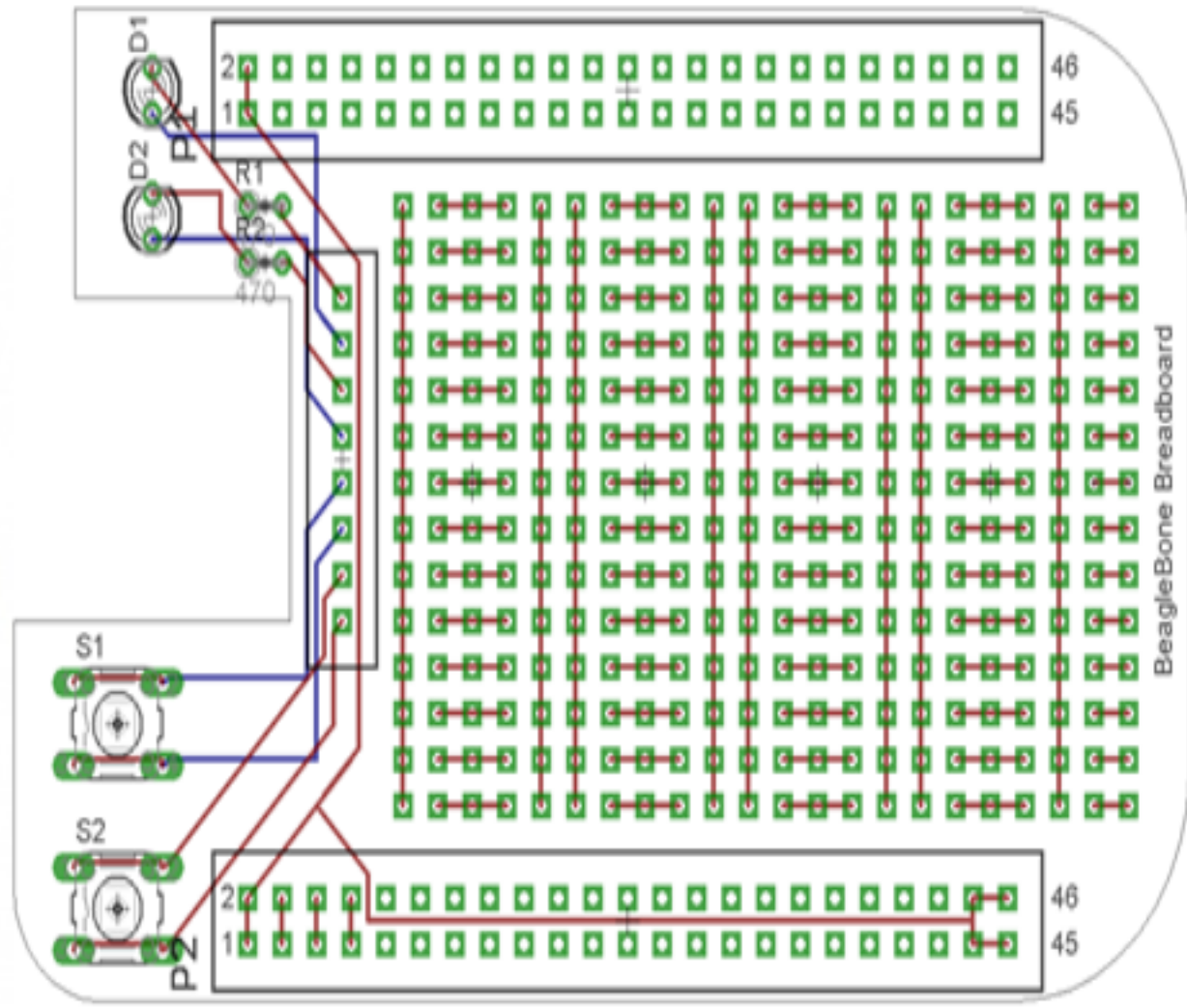
closed Gnd
Low

ANOTHER GOOD SOLUTION



THE LAB CAPE





SCHEMATIC

LAB CAPE S

P1

GPIO1_6	3	4	GPIO1_7
GPIO1_2	5	6	GPIO1_3
TIMER4	7	8	TIMER7
TIMER5	9	10	TIMER6
GPIO1_13	11	12	GPIO1_12
EHRPWM2B	13	14	GPIO1_26
GPIO1_15	15	16	GPIO1_14
GPIO1_27	17	18	GPIO2_1
EHRPWM2A	19	20	GPIO1_31
GPIO1_30	21	22	GPIO1_5
GPIO1_4	23	24	GPIO1_1
GPIO1_0	25	26	GPIO1_29
GPIO2_22	27	28	GPIO2_24
GPIO2_23	29	30	GPIO2_25
UART5_CTSN	31	32	UART5_RTSN
UART4_RTSN	33	34	UART3_RTSN
UART4_CTSN	35	36	UART3_CTSN
UART5_TXD	37	38	UART5_RXD
GPIO_12	39	40	GPIO2_13
GPIO2_10	41	42	GPIO2_11
GPIO2_8	43	44	GPIO2_9
GPIO2_6	45	46	GPIO2_7

FEMALE HEADER 2x23

DGND DGND

P2

VDD_3V3EXP	3	4	VDD_3V3EXP
VDD_5V	5	6	VDD_5V
SYS_5V	7	8	SYS_5V
PWR_BUT	9	10	SYS_RESETN
UART4_RXD	11	12	GPIO1_28
UART4_TXD	13	14	EHRPWM1A
UART3_RXD	15	16	EHRPWM1B
I2C1_SCL	17	18	I2C1_SDA
I2C2_SCL	19	20	I2C2_SDA
UART2_TXD	21	22	UART2_RXD
UART3_TXD	23	24	UART1_TXD
GPIO3_21	25	26	UART1_RXD
GPIO3_19	27	28	SPI1_CS0
SPI1_D0	29	30	SPI1_D1
SPI1_SCLK	31	32	VDD_ADC
AIN4	33	34	
AIN6	35	36	AIN5
AIN2	37	38	AIN3
AIN0	39	40	AIN1
CLKOUT2	41	42	GPIO0_7
	43	44	
	45	46	

FEMALE HEADER 2x23

AGND

DGND DGND

P3

8-PIN HEADER

470 R1 D1

470 R2 D2

S1

S2

TH1 TH2 TH3 TH4

TH5 TH6 TH7 TH8

TH9 TH10

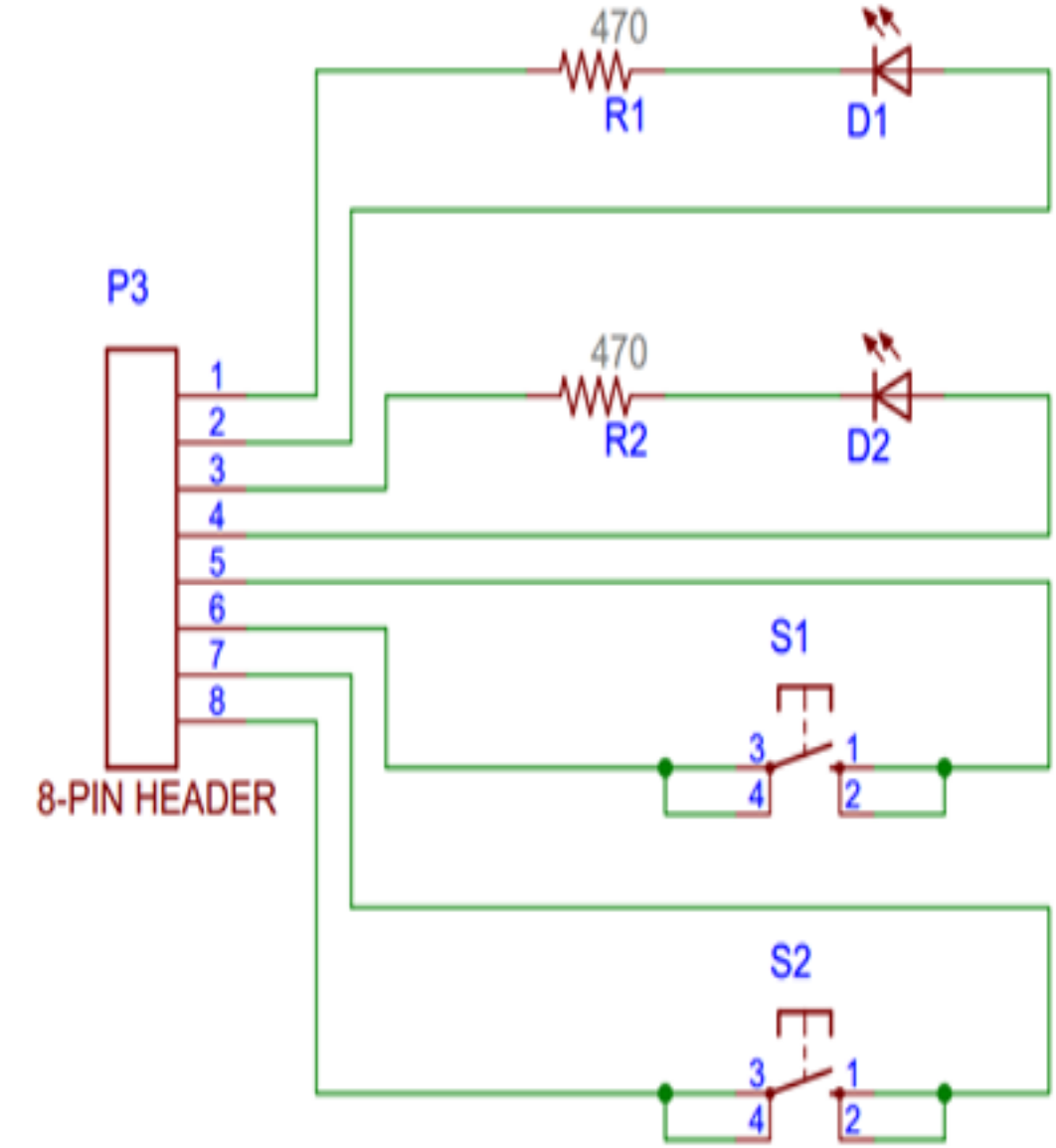
TITLE: Proto

Document Number:

REV:

MSOE UNIVERSITY

LAB CAPE SCHEMATIC



ITM	QTY	REF	PART	DESCRIPTION	DISTR	PART #
1	1		PCB	2-LAYER 3.4" x 2.15"		
2	2	P1, P2	2x23 HDR FE	DUAL - STRAIGHT SOCKET STRIP .025" SQ. PINS	MLE	SSHQ-123-D-08-F-LF
3	1	P3	8 PIN HDR FE	CONN HEADER FEMALE 8 POS 0.1" GOLD	DK	PPPC081LFBN-RC
4	2	S1, S2	BUTTONS	SWITCH TACT SPST-NO .05A 24V	DK	B3F-1000
5	2	D1, D2	LEDS	LED GREEN 3MM 568NM 20mA 2.12V	DK	WP7104SGC
6	2	R1, R2	RESISTOR	RES 470 OHM 1/4W 5% CF MINI	DK	CFM14JT470R
7	1	BR1	BREADBOARD	WHT ADHSV SLDRLSS BRDBRD 170 TIE PT 1.8" x 1.37"	PLU	1490
8	1		JMPR WIRE KIT	10 x 14 LNGTH .1" .2" .3" .4" .5" .6" .7" .8" .9" 1" 2" 3" 4" 5"	SQR	

THE SCHEMATIC WE BUILT WITH THE PULL UP RESISTOR