



Division

Lecture Objectives:

- 1) Perform binary division of two numbers.
- 2) Define dividend, divisor, quotient, and remainder.
- 3) Explain how division is accomplished in computer hardware.
- 4) Construct a simple program which uses MIPS integer multiplication and division.

Friday & fun :-)

⇒ Exam

One 8.5 x 11 sheet of notes.

- Review sheet online.

→ 5 minutes going over sheet back
questions

Questions:

DSP's
ATMEGA32

Harvard V3 Von Neuman
Different

Word Sizes

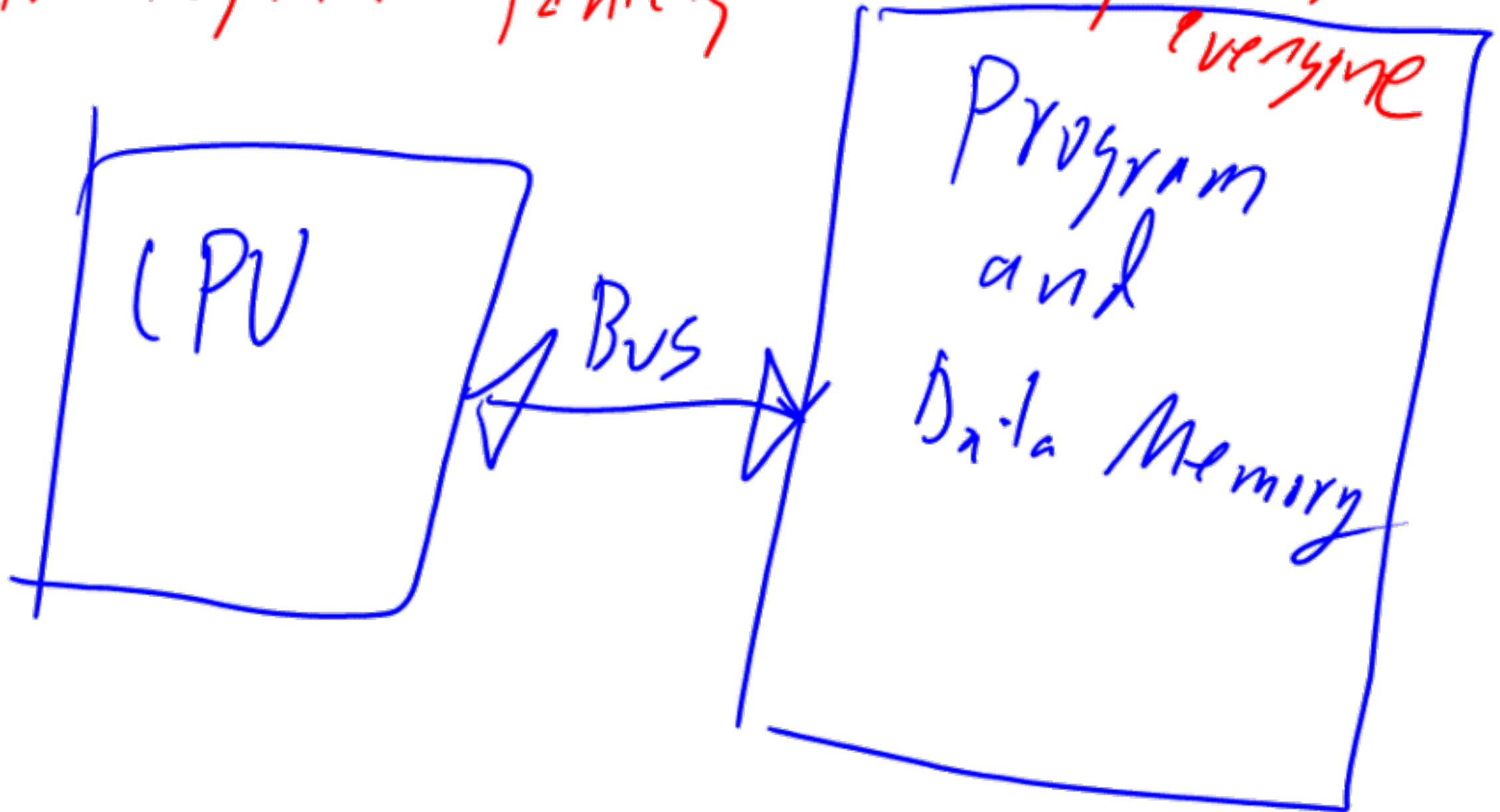
Harvard

Where
the variables
live



Von Neumann

MIPS, ARM, Intel, Motorola, almost everyone



$\boxed{-5} \Rightarrow 2$'s Complement

$|5| \Rightarrow 0000101 \Rightarrow 5$

\Rightarrow Complement it 11111010

\Rightarrow Add one $\underline{11111011} \Rightarrow -5$ in
2's Complement

Equations \Rightarrow Good to write on
note sheet.

Packet/Sheet of Maps

Instructions will be provided.

Big Vs Lil Endian

Most Significant Byte

32 bits

32 bit value: 0x013468AB

A B

Little Endian Big Endian

0x03	01
0x02	34
0x01	68
0x00	AB

0x03	AB
0x02	68
0x01	34
0x00	01

4 bytes

Least Significant Byte

NOR:

A always @ 7erd

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Same thing

Not

Pseudo input

A	C
0	1
1	0

Definitions (Pg 237)

- Dividend
 - The first operand of a divide operation ✓
- Divisor
 - The second operand of a divide operation ✓
- Quotient
 - The final result of a divide operation ✓
- Remainder
 - The second result to a division operation ✓

→ % Modulus

Division (Long Approach)

- Solve the following

$$\begin{array}{r} 8 \overline{) 740} \\ \underline{72} \\ 20 \\ \underline{16} \\ 4 \end{array}$$

092 R 4

Quotient
—
Remainder

Division Algorithm

- Check for 0 divisor — *Impossible / infinity*
- Long division approach
 - If divisor \leq dividend bits —
 - 1 bit in quotient, subtract
 - Otherwise
 - 0 bit in quotient, bring down next dividend bit
- Restoring division —
 - Do the subtract, and if remainder goes < 0, add divisor back
- Signed division
 - Divide using absolute values
 - Adjust sign of quotient and remainder as required

$2 \overline{) 18}$
Unsigned
#1's

$01001 \rightarrow (9)$
 $10 \overline{) 10010}$
 10
 $\underline{\quad}$
 00010
 10
 $\underline{\quad}$
 00
18

~~Both~~ Quotient \Rightarrow } Both
Remainder \Rightarrow } placed
in registers.

$$\sqrt[5]{27}$$

$$\begin{array}{r} 16 \quad 8 \quad 2 \quad 1 \\ 1 \quad 1 \quad 0 \quad 1 \end{array}$$

$$0101$$

$$\boxed{101} R \boxed{010}$$

$$0101 \overline{) 11011}$$

$$101$$

$$00111$$

$$101$$

$$010$$

$$5R2$$

Time is related to
how big the H 's are.

Faster Division

- Can't use parallel hardware as in multiplier
 - Subtraction is conditional on sign of remainder
- Faster dividers (e.g. SRT division) generate multiple quotient bits per step
 - Still require ~~multiple steps~~

MIPS Division

- Use HI/LO registers for result
 - HI: 32-bit remainder
 - LO: 32-bit quotient
 - Instructions
 - `div rs, rt` / `divu rs, rt`
 - No overflow or divide-by-0 checking
 - Software must perform checks if required
 - Use `mghi`, `mflo` to access result
- Handwritten notes:* "Signed" with arrows pointing to `div` and `divu`; "Unsigned" with an arrow pointing to `divu`.

Category	Instruction	Example	Meaning	Comments
Arithmetic	add	add \$s1,\$s2,\$s3	$\$s1 = \$s2 + \$s3$	Three operands; overflow detected
	subtract	sub \$s1,\$s2,\$s3	$\$s1 = \$s2 - \$s3$	Three operands; overflow detected
	add immediate	addi \$s1,\$s2,100	$\$s1 = \$s2 + 100$	+ constant; overflow detected
	add unsigned	addu \$s1,\$s2,\$s3	$\$s1 = \$s2 + \$s3$	Three operands; overflow undetected
	subtract unsigned	subu \$s1,\$s2,\$s3	$\$s1 = \$s2 - \$s3$	Three operands; overflow undetected
	add immediate unsigned	addiu \$s1,\$s2,100	$\$s1 = \$s2 + 100$	+ constant; overflow undetected
	move from coprocessor register	mfc0 \$s1,\$epc	$\$s1 = \epc	Copy Exception PC + special regs
	multiply	mult \$s2,\$s3	Hi, Lo = $\$s2 \times \$s3$	64-bit signed product in Hi, Lo
	multiply unsigned	multu \$s2,\$s3	Hi, Lo = $\$s2 \times \$s3$	64-bit unsigned product in Hi, Lo
	divide	div \$s2,\$s3	Lo = $\$s2 / \$s3$, Hi = $\$s2 \bmod \$s3$	Lo = quotient, Hi = remainder
divide unsigned	divu \$s2,\$s3	Lo = $\$s2 / \$s3$, Hi = $\$s2 \bmod \$s3$	Unsigned quotient and remainder	
	move from Hi	mfhi \$s1	$\$s1 = \text{Hi}$	Used to get copy of Hi
	move from Lo	mflo \$s1	$\$s1 = \text{Lo}$	Used to get copy of Lo
Data transfer	load word	lw \$s1,20(\$s2)	$\$s1 = \text{Memory}[\$s2 + 20]$	Word from memory to register
	store word	sw \$s1,20(\$s2)	$\text{Memory}[\$s2 + 20] = \$s1$	Word from register to memory
	load half unsigned	lhu \$s1,20(\$s2)	$\$s1 = \text{Memory}[\$s2 + 20]$	Halfword memory to register
	store half	sh \$s1,20(\$s2)	$\text{Memory}[\$s2 + 20] = \$s1$	Halfword register to memory
	load byte unsigned	lbu \$s1,20(\$s2)	$\$s1 = \text{Memory}[\$s2 + 20]$	Byte from memory to register
	store byte	sb \$s1,20(\$s2)	$\text{Memory}[\$s2 + 20] = \$s1$	Byte from register to memory
	load linked word	ll \$s1,20(\$s2)	$\$s1 = \text{Memory}[\$s2 + 20]$	Load word as 1st half of atomic swap
	store conditional word	sc \$s1,20(\$s2)	$\text{Memory}[\$s2 + 20] = \$s1; \$s1 = 0$ or 1	Store word as 2nd half atomic swap
	load upper immediate	lui \$s1,100	$\$s1 = 100 * 2^{16}$	Loads constant in upper 16 bits
Logical	AND	AND \$s1,\$s2,\$s3	$\$s1 = \$s2 \& \$s3$	Three reg. operands; bit-by-bit AND
	OR	OR \$s1,\$s2,\$s3	$\$s1 = \$s2 \$s3$	Three reg. operands; bit-by-bit OR
	NOR	NOR \$s1,\$s2,\$s3	$\$s1 = \sim (\$s2 \$s3)$	Three reg. operands; bit-by-bit NOR
	AND immediate	ANDI \$s1,\$s2,100	$\$s1 = \$s2 \& 100$	Bit-by-bit AND with constant
	OR immediate	ORI \$s1,\$s2,100	$\$s1 = \$s2 100$	Bit-by-bit OR with constant
	shift left logical	sll \$s1,\$s2,10	$\$s1 = \$s2 \ll 10$	Shift left by constant
	shift right logical	srl \$s1,\$s2,10	$\$s1 = \$s2 \gg 10$	Shift right by constant
Conditional branch	branch on equal	beq \$s1,\$s2,25	if ($\$s1 == \$s2$) go to PC + 4 + 100	Equal test; PC-relative branch
	branch on not equal	bne \$s1,\$s2,25	if ($\$s1 != \$s2$) go to PC + 4 + 100	Not equal test; PC-relative
	set on less than	slt \$s1,\$s2,\$s3	if ($\$s2 < \$s3$) $\$s1 = 1$; else $\$s1 = 0$	Compare less than; two's complement
	set less than immediate	slti \$s1,\$s2,100	if ($\$s2 < 100$) $\$s1 = 1$; else $\$s1 = 0$	Compare < constant; two's complement
	set less than unsigned	sltu \$s1,\$s2,\$s3	if ($\$s2 < \$s3$) $\$s1 = 1$; else $\$s1 = 0$	Compare less than; natural numbers
	set less than immediate unsigned	sltiu \$s1,\$s2,100	if ($\$s2 < 100$) $\$s1 = 1$; else $\$s1 = 0$	Compare < constant; natural numbers
Unconditional jump	jump	j 2500	go to 10000	Jump to target address
	jump register	jr \$ra	go to \$ra	For switch, procedure return
	jump and link	jal 2500	$\$ra = \text{PC} + 4$; go to 10000	For procedure call

Instructions we've talked about thus far

Procedure MIPS

Multiply
Division
Specific



In Class Example

- Lets write an assembly program which will perform the following:
 - Read two integer numbers from the user
 - Print out their product
 - Print out their quotient
 - Print out the remainder (If the numbers are not evenly divisible)